

# Compal Confidential

## AAP11/AAP21

### Schematic Document

# WWW.AITECH1.RU

SKL-H platform with ALMP Magneto dGPU

Rev: 1.0(A00) PVT

2015/07/21

@ : Nopop Component

DIS@ : Discrete Part

EMI@ /@EMI@ : EMI pop/unpop part

ESD@ /@ESD@ : ESD pop/unpop part

RF@ /@RF@ : RF pop/unpop part

CONN@ : Connector Component

AOAC@ : Intel AOAC

DS3/NODS3: deepS3

TBT@: ThunderBolt

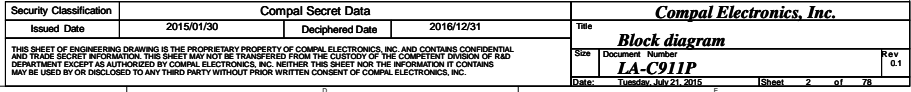
PD@: Power Delivery

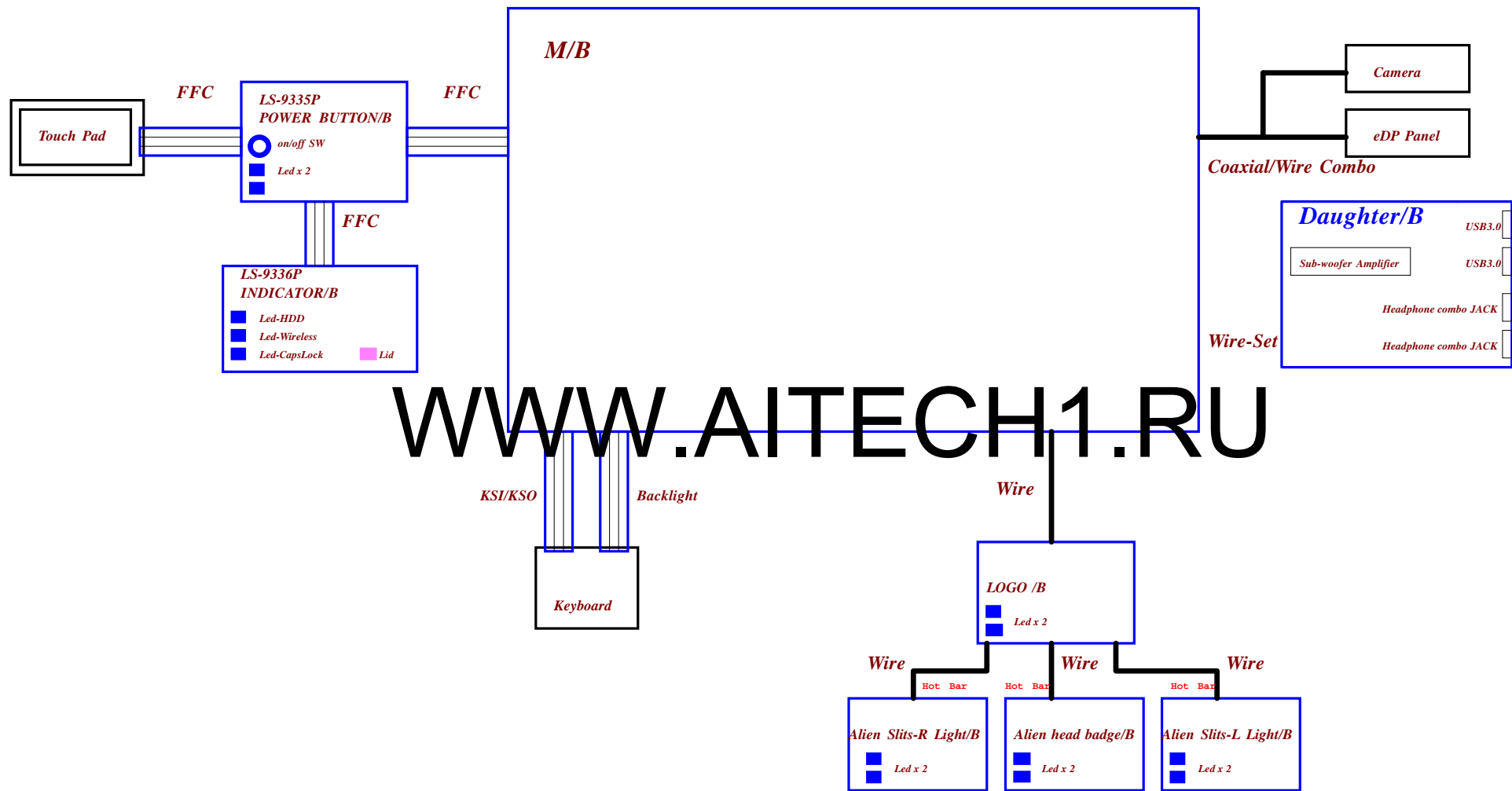
DAX PCB  
DAZ18F00100  
PCB 18F LA-B752P REV0 M/B 8  
R1@

DAX PCB  
DAZ18F00101  
PCB 18F LA-B752P REV0 M/B 8  
R3@

12L

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Issued Date	2015/01/30	Deciphered Date	2016/12/31	Title Cover Sheet		
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Board ID Table for AD channel

Vcc	3.3V +/- 1%					
Ra	100K +/- 1%					
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3	
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B	NVIDIA Graphic
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B	
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46	
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76	AMD Graphic
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96	
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7	
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0	
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC	
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6	
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF	

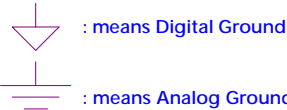
Board ID TABLE

ID		PCB Revision
NV	AMD	
0	10	EVT-1
1	11	DVT-1
2	12	DVT-2
3	13	DVT-3
4	14	Pilot build

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CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100/1000 LAN
CLKOUT_PCIE3	M.2 Card WLAN
CLKOUT_PCIE4	dGPU (N15P)
CLKOUT_PCIE5	DGPU (Caldera)

Symbol Note :



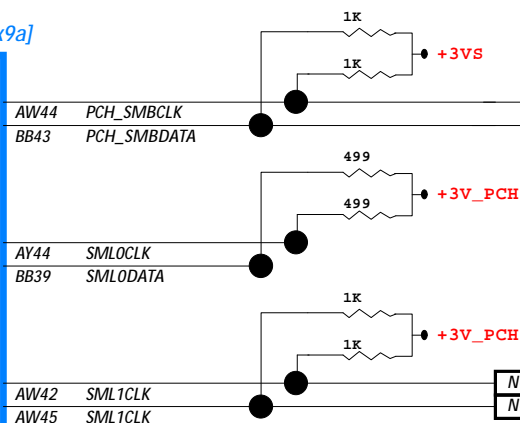
USB3.0

Port1	Right side1
Port2	Right side2
Port3	Left side 1
Port4	
Port5	Caldera
Port6	Left side 2
USB2.0	
Port0	Right side1
Port1	Left side 1 (PowerShare)
Port2	Caldera
Port3	ELC
Port4	BT
Port5	Touch screen
Port6	Camera
Port7 / 8	Right side 2 Left side 2
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100/1000 LAN
Lane 4	M.2 Card WLAN
Lane 5	PCIE 4x MUX
Lane 6	
SATA	
SATA0	HDD
SATA1	NGFF SSD
SATA2	NGFF SSD
SATA3	

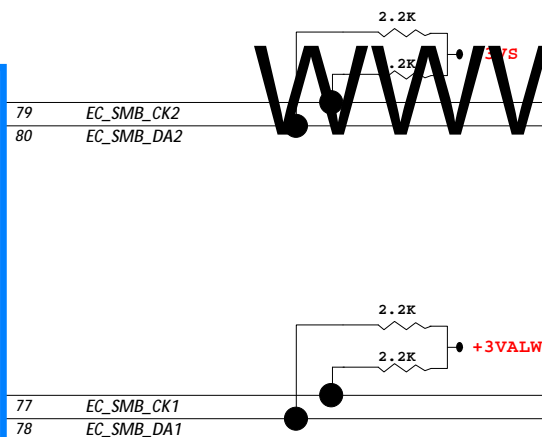
SMBUS Address [0x9a]



Skylake



KBC  
KB9022QD



CPU,C  
DDR,D  
GPU,DP,HDMI,EDP,V  
LAN,L  
AUDIO,A  
NGFF,N  
USB,U  
CALDERA,M  
HDD,S  
ELC,E  
FAN,F  
TP,T  
KBC,K  
DC,O

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253 DIMMA  
254 SMBUS Address [A0]

253 DIMMB  
254 SMBUS Address [A4]

4 FFS  
6 SMBUS Address [1Dh]

5 JTP  
6 SMBUS Address [TBD]

U2407 Thermal Sensor  
SMBUS Address [0x9A]

UT4 TBT  
SMBUS Address [0x7]

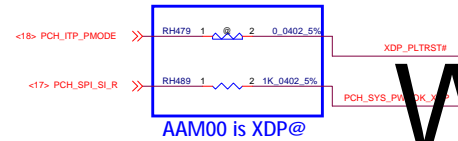
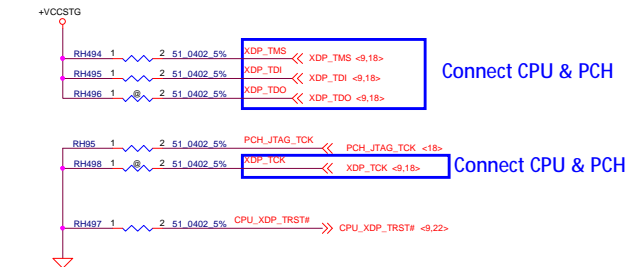
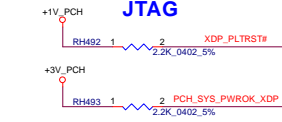
SMBUS Address [0x9E]

SMBUS Address [0x12]

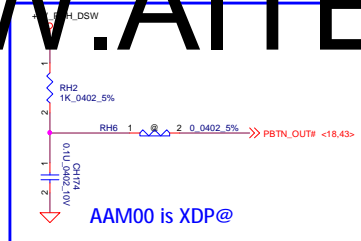
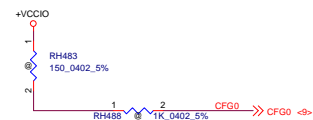
SMBUS Address [0x16]

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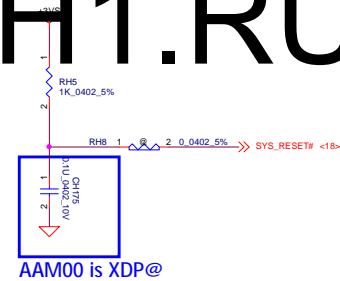
# JTAG



AAM00 is XDP@



AAM00 is XDP@



AAM00 is XDP@

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<14> DDR\_A\_D[0..63]  
<14> DDR\_A\_MA[0..13]  
<14> DDR\_A\_DQS#[0..7]  
<14> DDR\_A\_DQS[0..7]

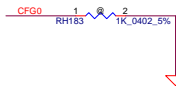


Security Classification		Compal Secret Data			
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				Size	Rev
				Document Number	0.1
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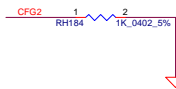


## CFG Straps for Processor

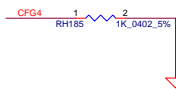
Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	<p>★ 1 = (Default) Normal Operation; No stall.</p> <p>0 = Stall.</p>



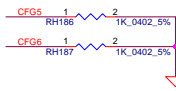
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	<p>1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>★ 0: Lane Reversed</p>



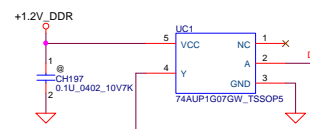
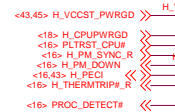
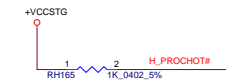
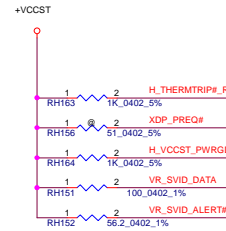
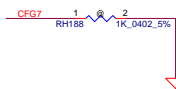
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



PCIe Port Bifurcation Straps	
CFG[6:5]	<p>11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>★ 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>

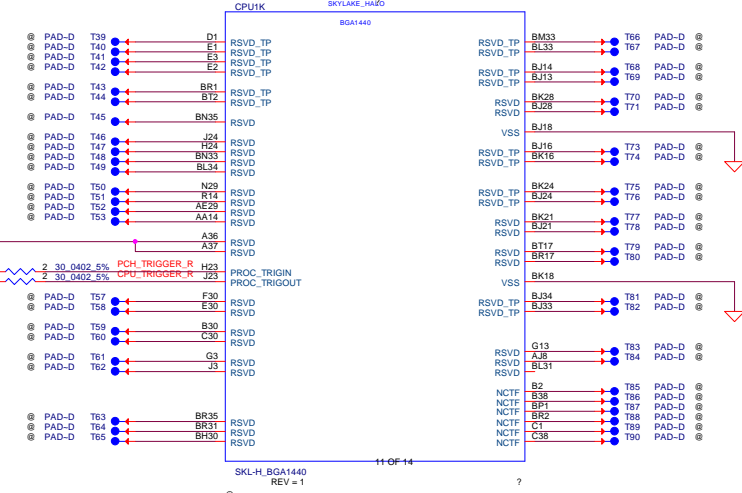


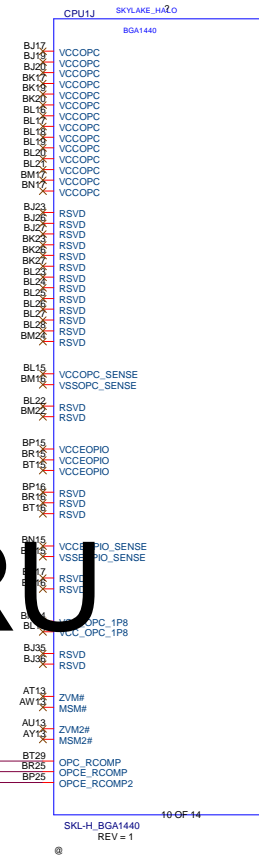
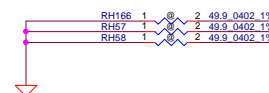
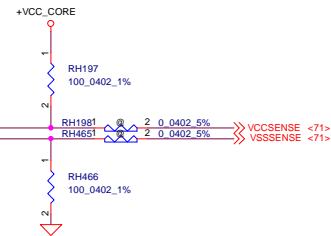
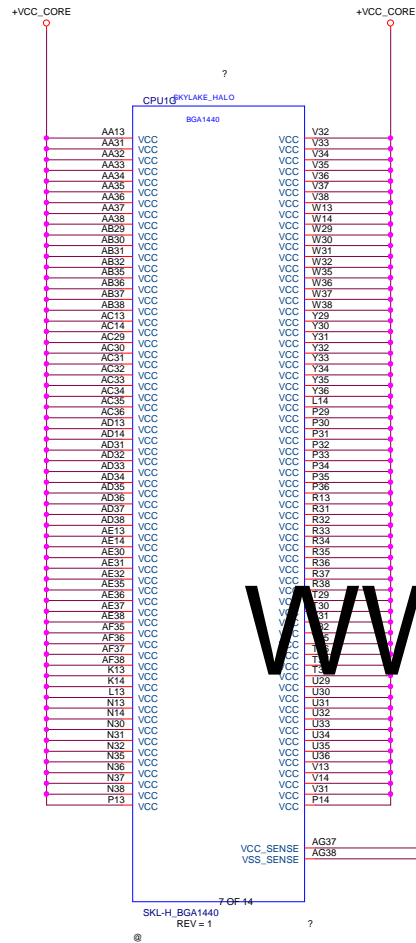
PEG DEFER TRAINING	
CFG7	<p>★ 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>



4/13 UCL SA00005U600 is X1 code.  
Change PN SA00005U600 to SA00007WE00.

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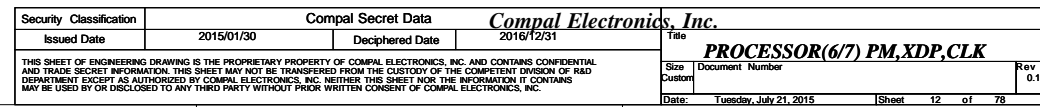


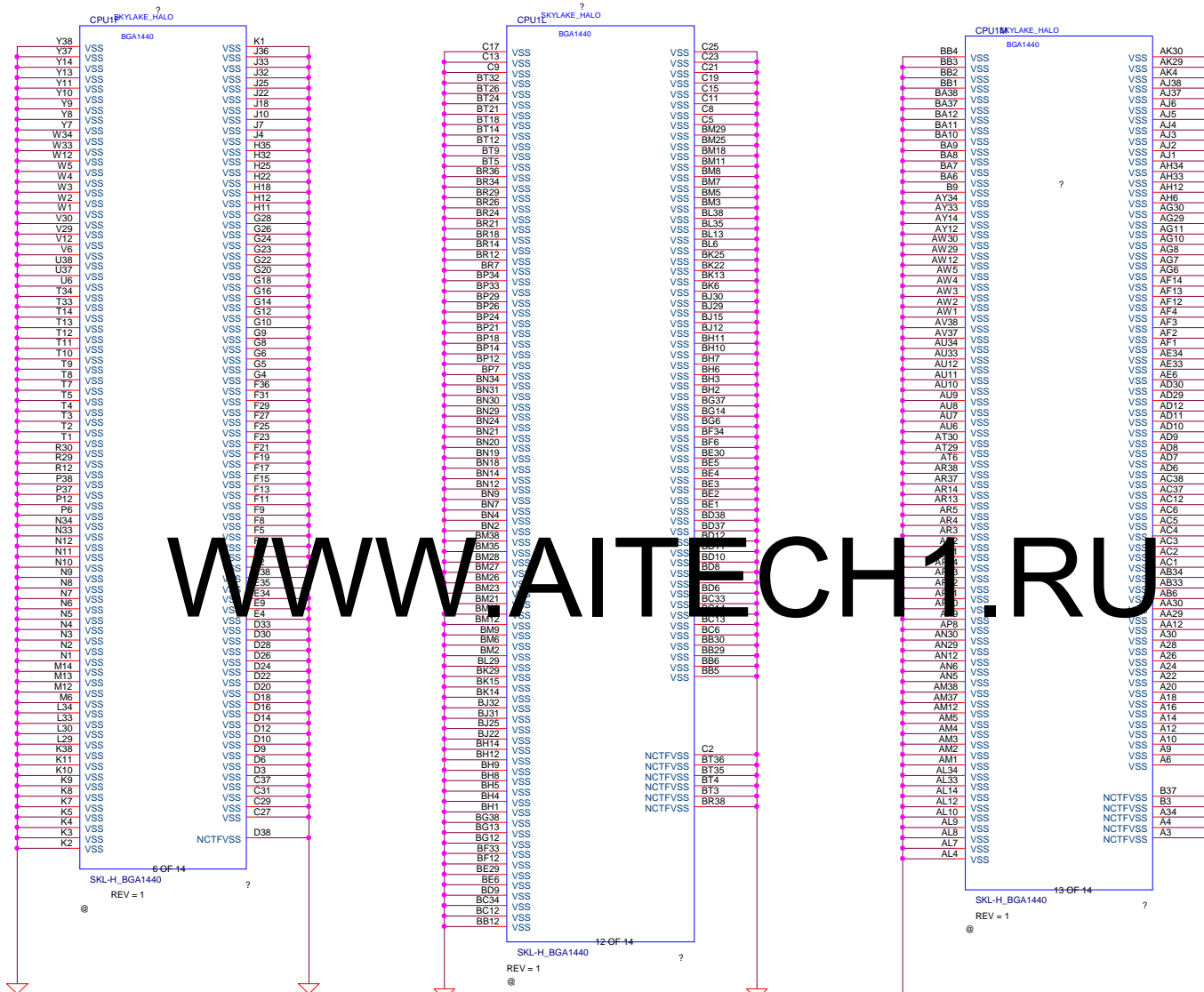


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PROCESSOR(4/7) PWR,BYPASS				Sheet	10 of 78
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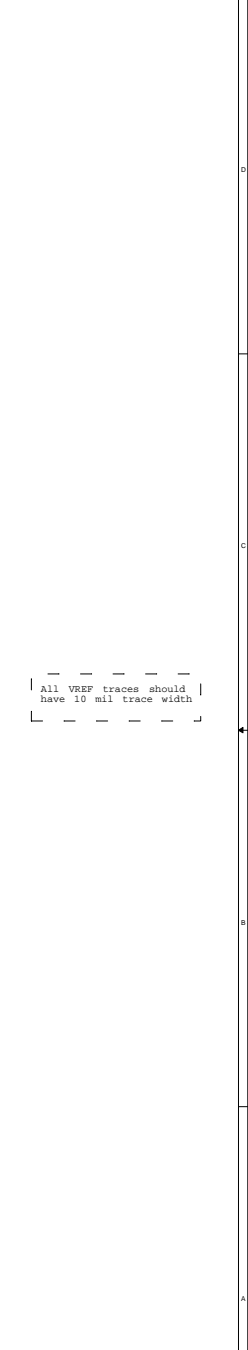
CET DFT Confindinal



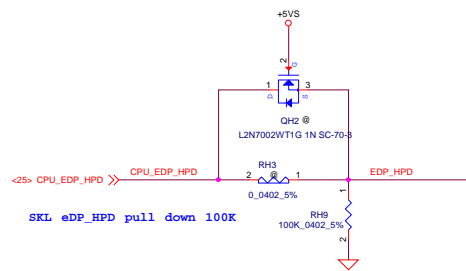
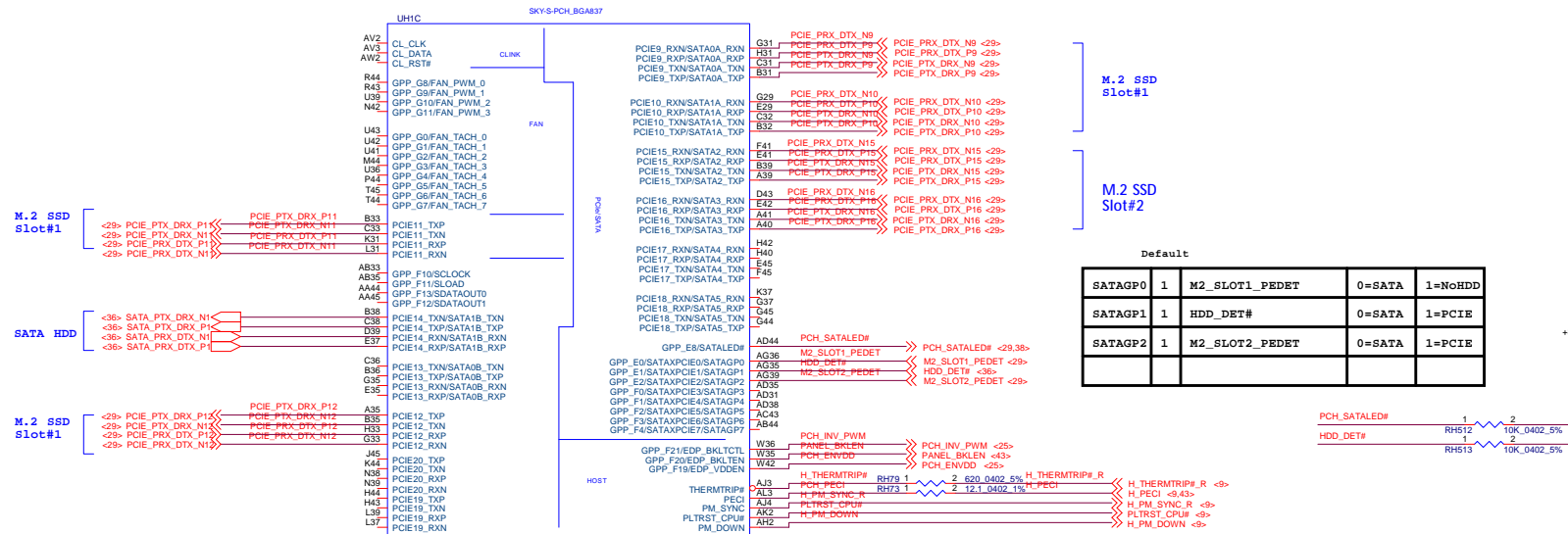


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						Size	Document Number		Rev	
						Custom			0.1	
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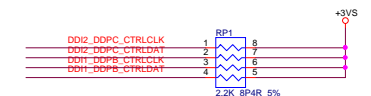
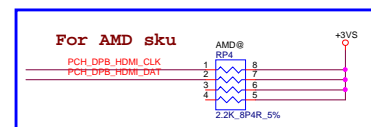
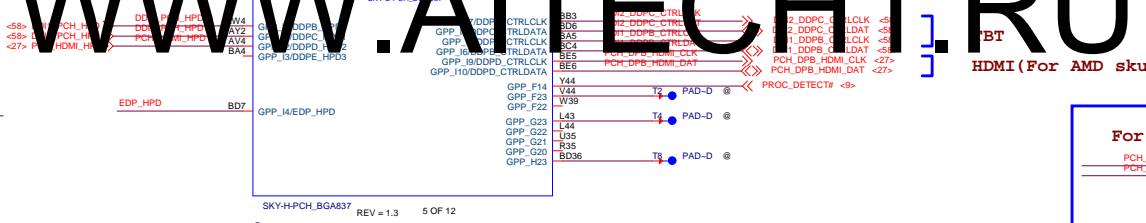




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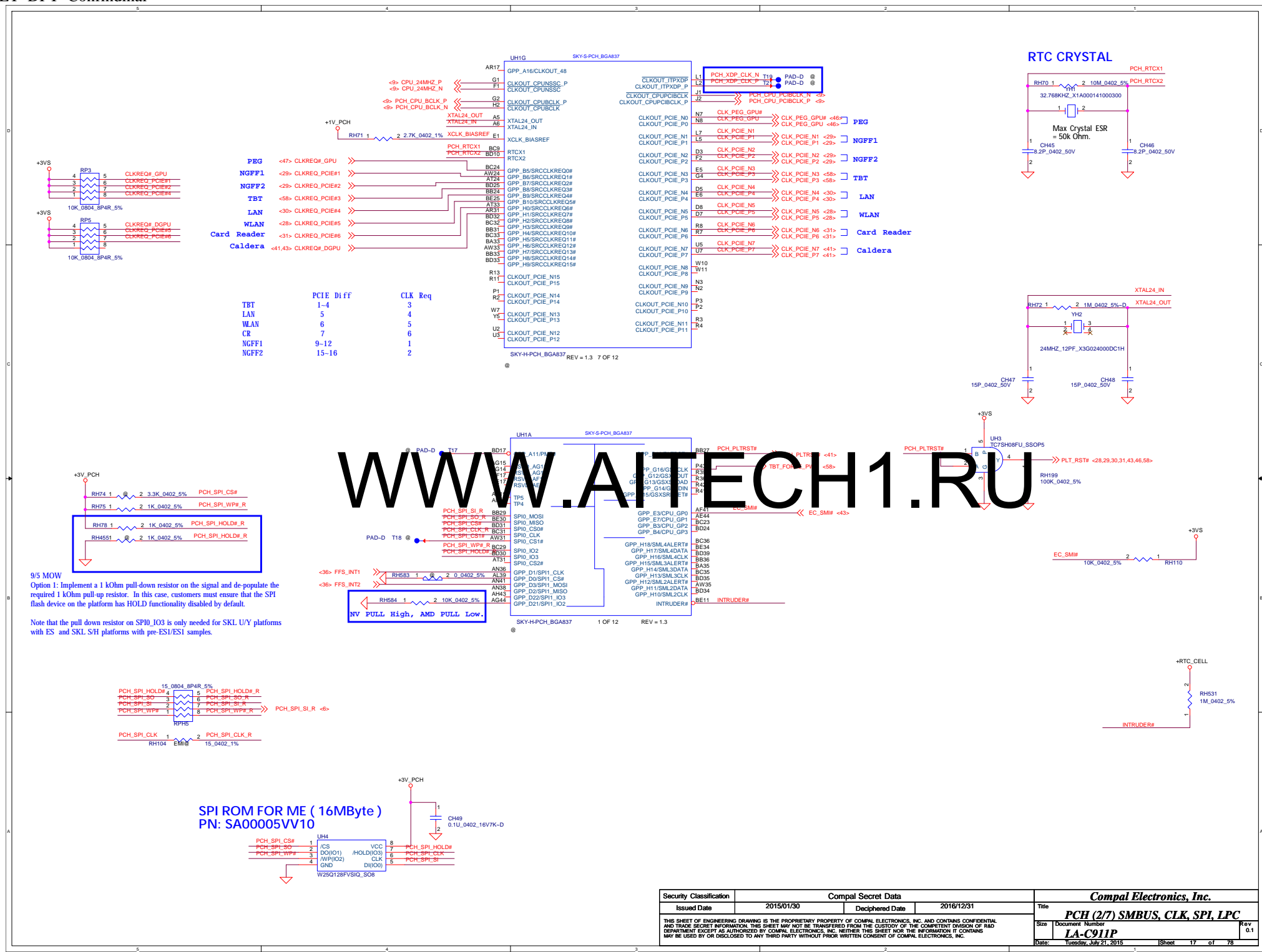


## PCH Strap PIN

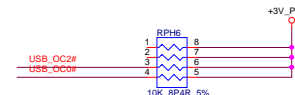
### DisplayPort® Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect





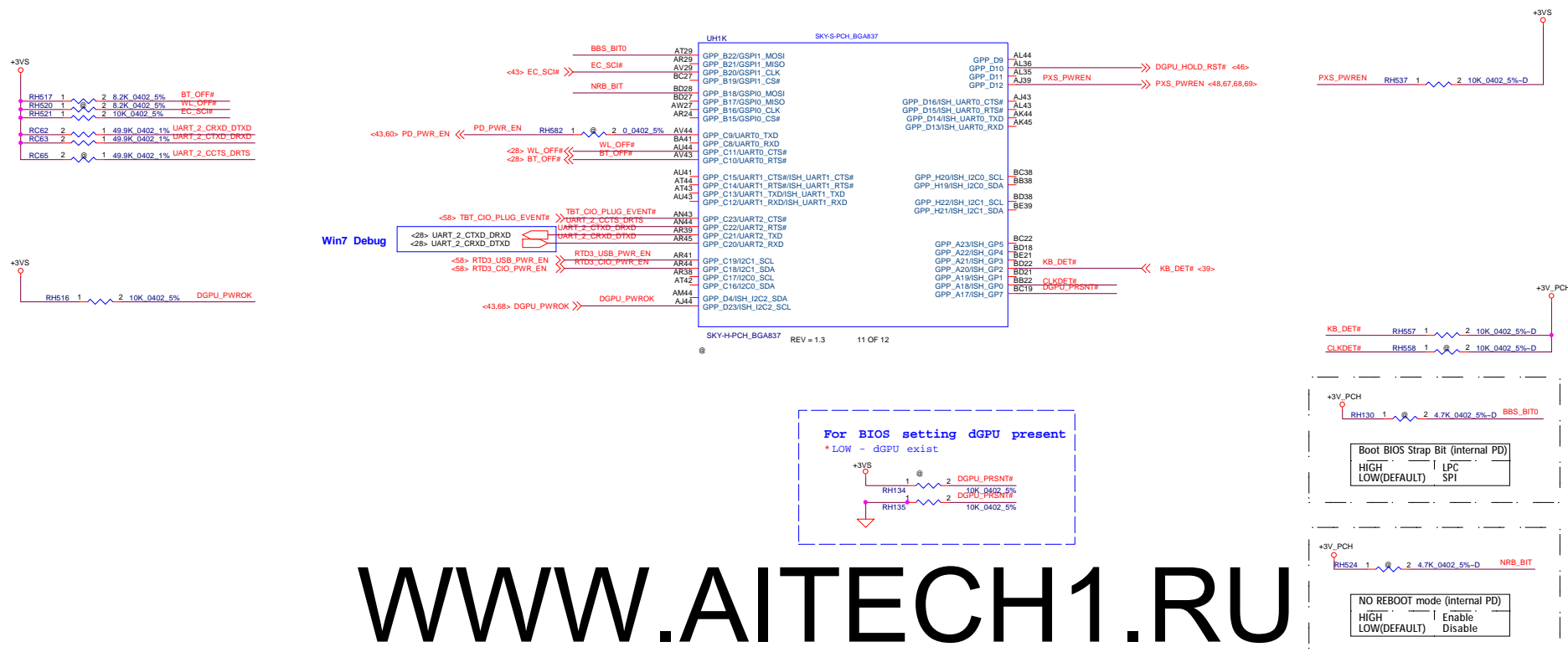




SHELL-PCH B08A



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				LA-C911P	Rev 0.1
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7	0.00	0.00	0.00
8	0.00	0.00	0.00
9	0.00	0.00	0.00
10	0.00	0.00	0.00
11	0.00	0.00	0.00
12	0.00	0.00	0.00
13	0.00	0.00	0.00
14	0.00	0.00	0.00
15	0.00	0.00	0.00
16	0.00	0.00	0.00
17	0.00	0.00	0.00
18	0.00	0.00	0.00
19	0.00	0.00	0.00
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28	0.00	0.00	0.00
29	0.00	0.00	0.00
30	0.00	0.00	0.00
31	0.00	0.00	0.00
32	0.00	0.00	0.00
33	0.00	0.00	0.00
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53	0.00	0.00	0.00
54	0.00	0.00	0.00
55	0.00	0.00	0.00
56	0.00	0.00	0.00
57	0.00	0.00	0.00
58	0.00	0.00	0.00
59	0.00	0.00	0.00
60	0.00	0.00	0.00
61	0.00	0.00	0.00
62	0.00	0.00	0.00
63	0.00	0.00	0.00
64	0.00	0.00	0.00
65	0.00	0.00	0.00
66	0.00	0.00	0.00
67	0.00	0.00	0.00
68	0.00	0.00	0.00
69	0.00	0.00	0.00
70	0.00	0.00	0.00
71	0.00	0.00	0.00
72	0.00	0.00	0.00
73	0.00	0.00	0.00
74	0.00	0.00	0.00
75	0.00	0.00	0.00
76	0.00	0.00	0.00
77	0.00	0.00	0.00
78	0.00	0.00	0.00
79	0.00	0.00	0.00
80	0.00	0.00	0.00
81	0.00	0.00	0.00
82	0.00	0.00	0.00
83	0.00	0.00	0.00
84	0.00	0.00	0.00
85	0.00	0.00	0.00
86	0.00	0.00	0.00
87	0.00	0.00	0.00
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89	0.00	0.00	0.00
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CET DFT Confindinal

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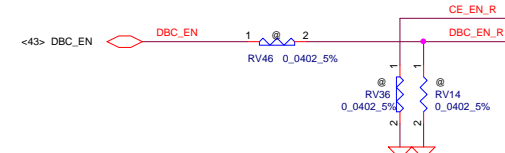
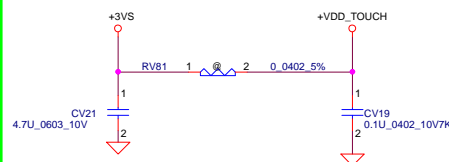
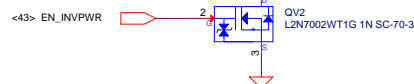
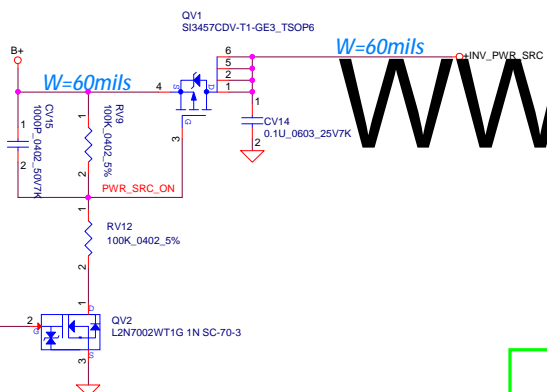
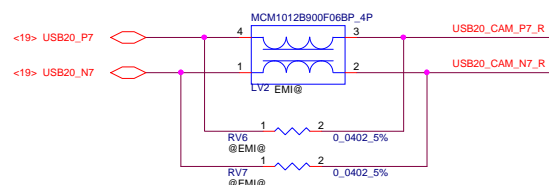
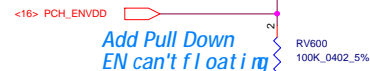
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				Size	Document Number
				LA-C911P	
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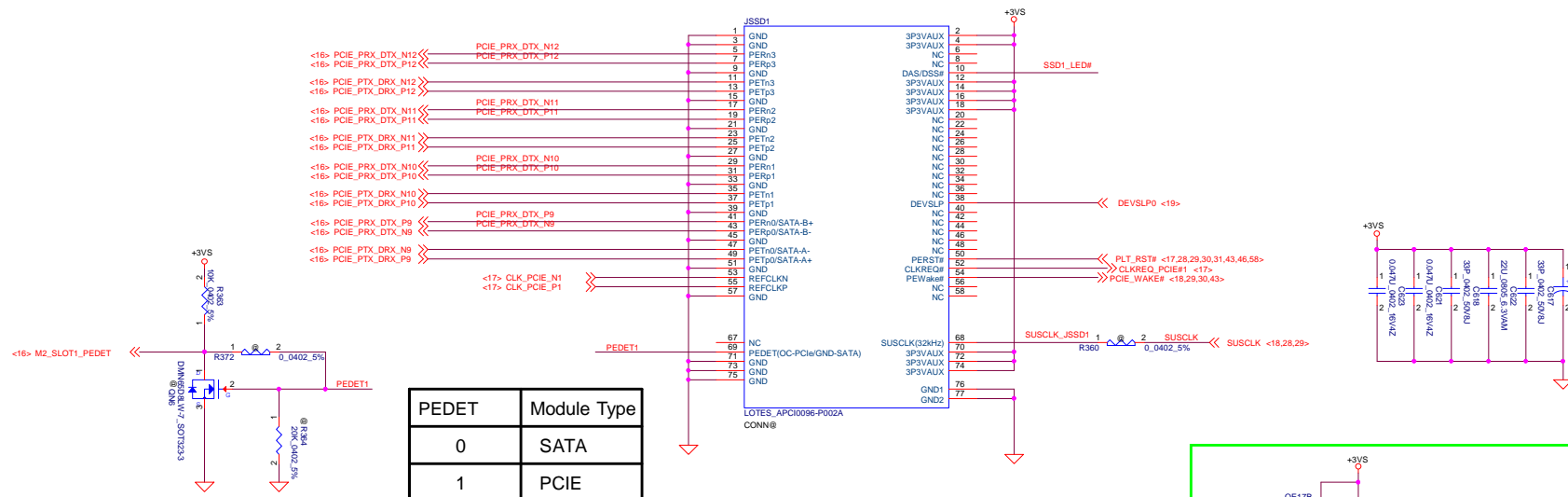
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				Size	Document Number	Rev
				Custom	LA-C911P	0.1
				Date:	Tuesday, July 21, 2015	Sheet 26 of 78

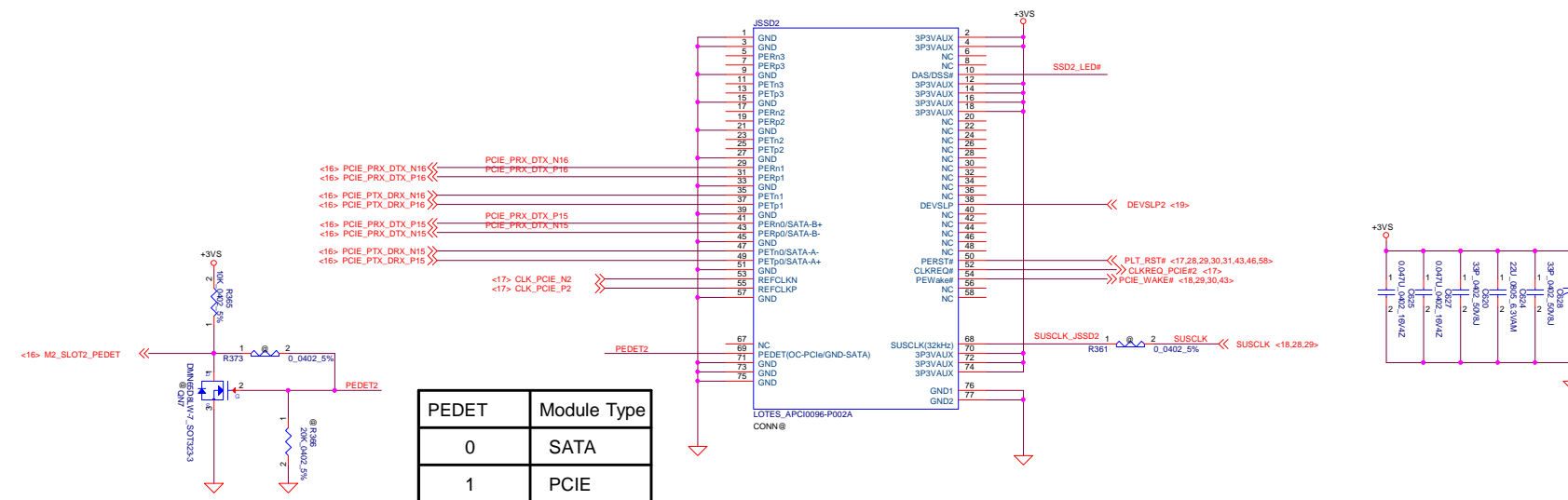




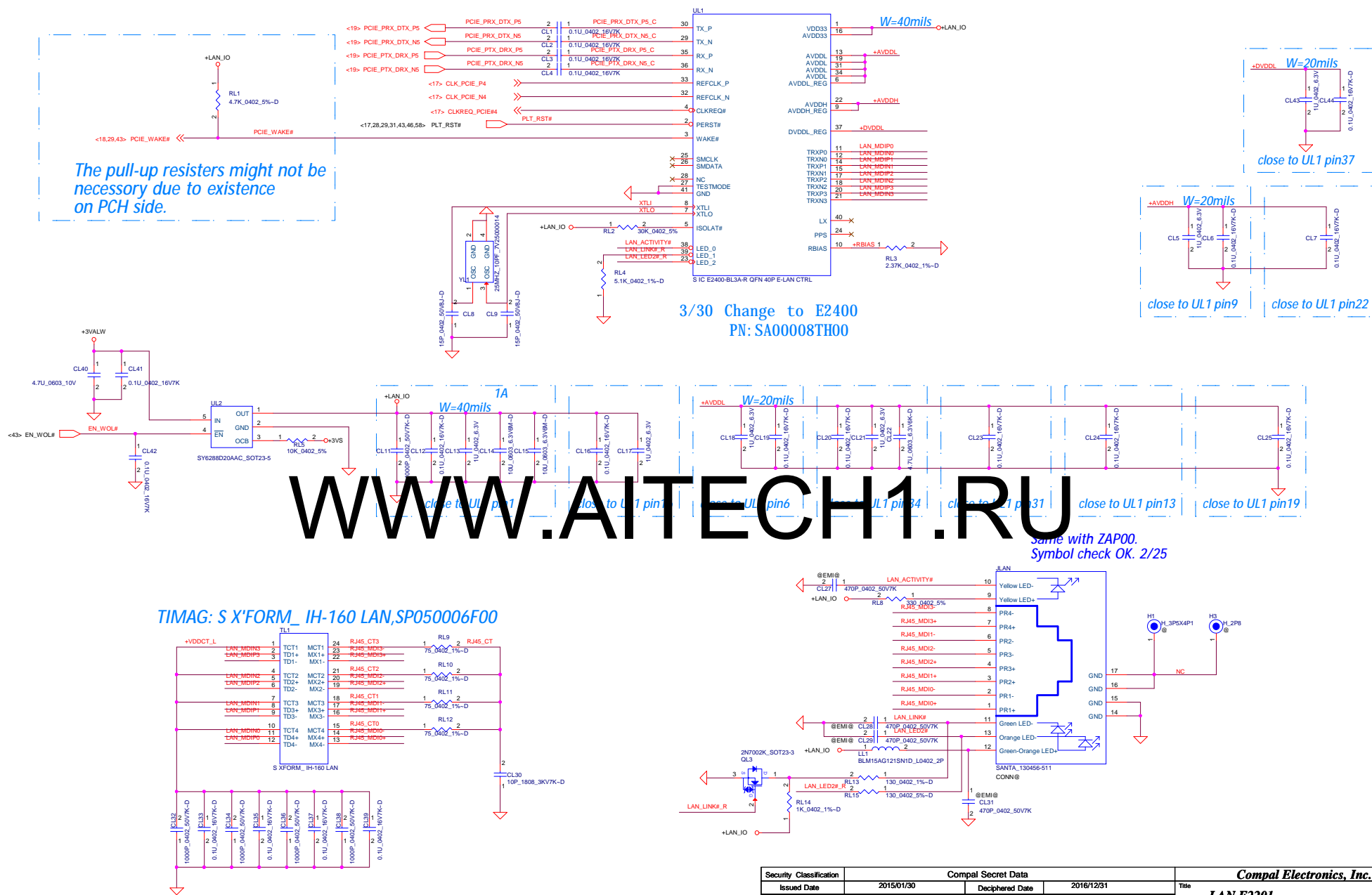
# SSD NGFF slot\_1 Key M



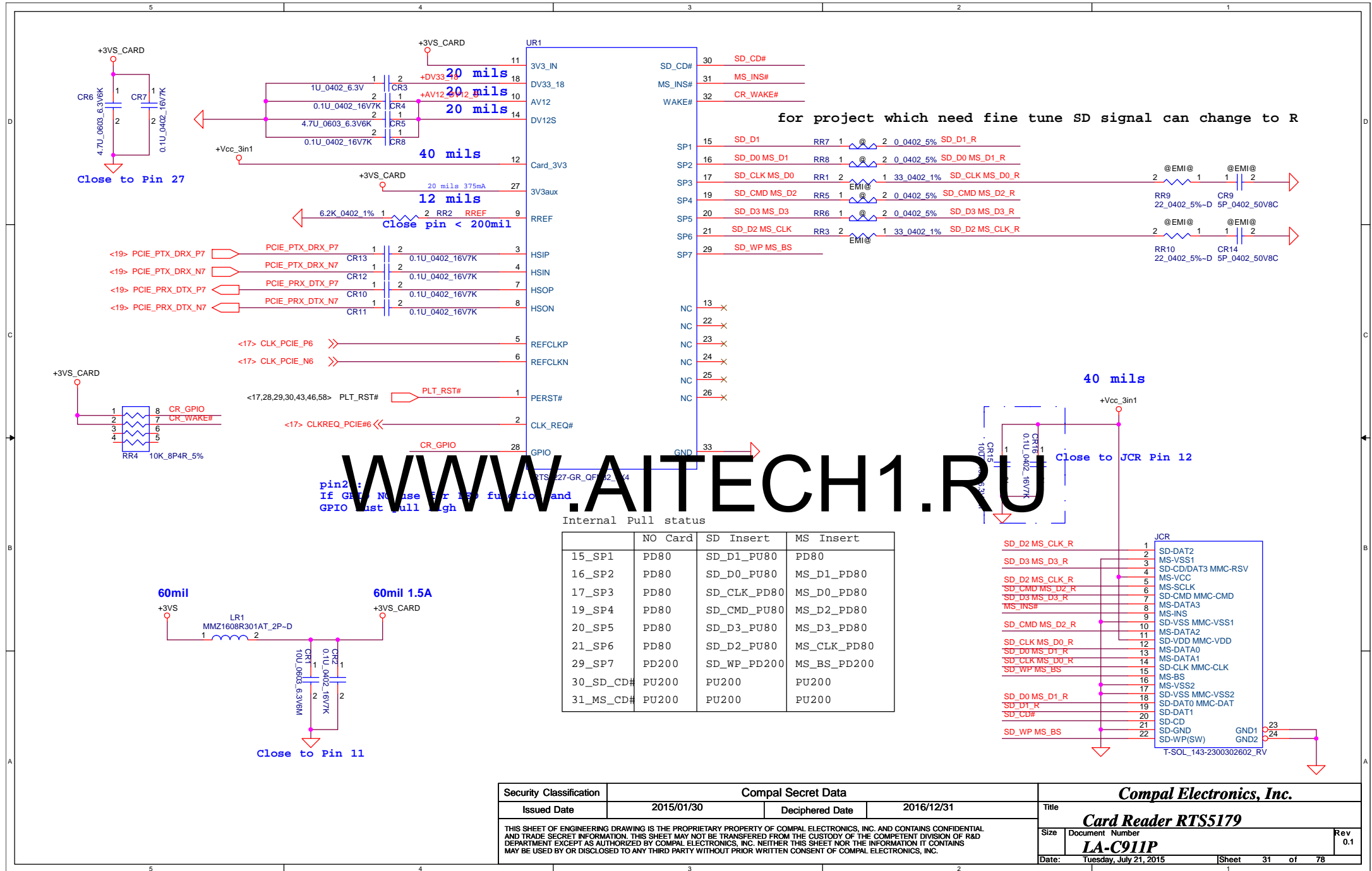
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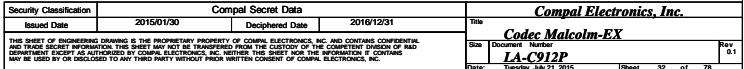


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Size	Document Number	Rev		0.1	
Date:	Tuesday, July 21, 2015	Sheet	30	of	76



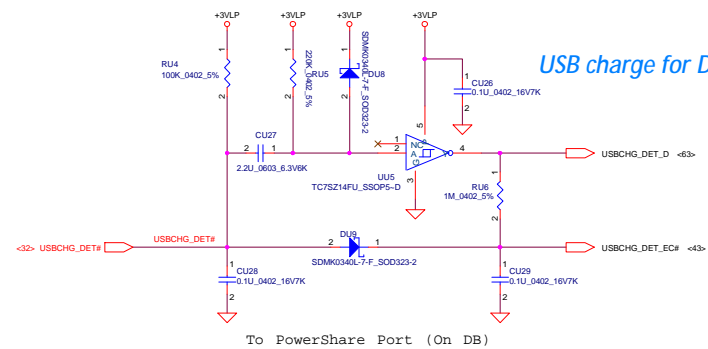
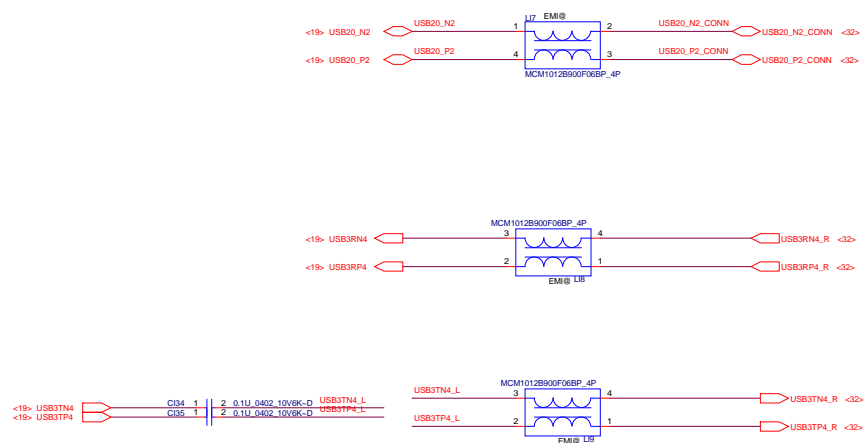




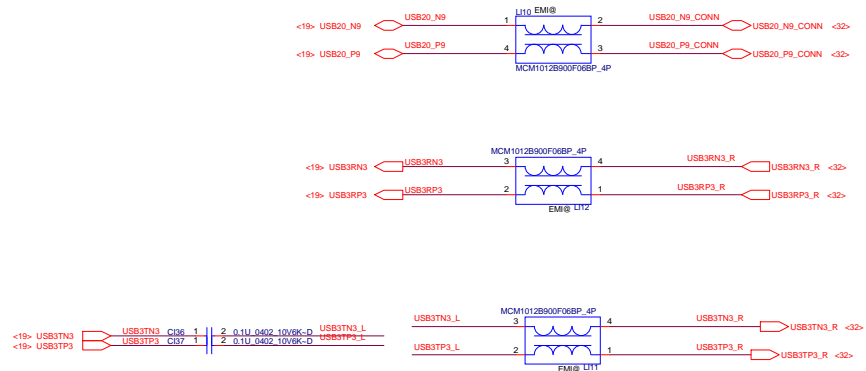
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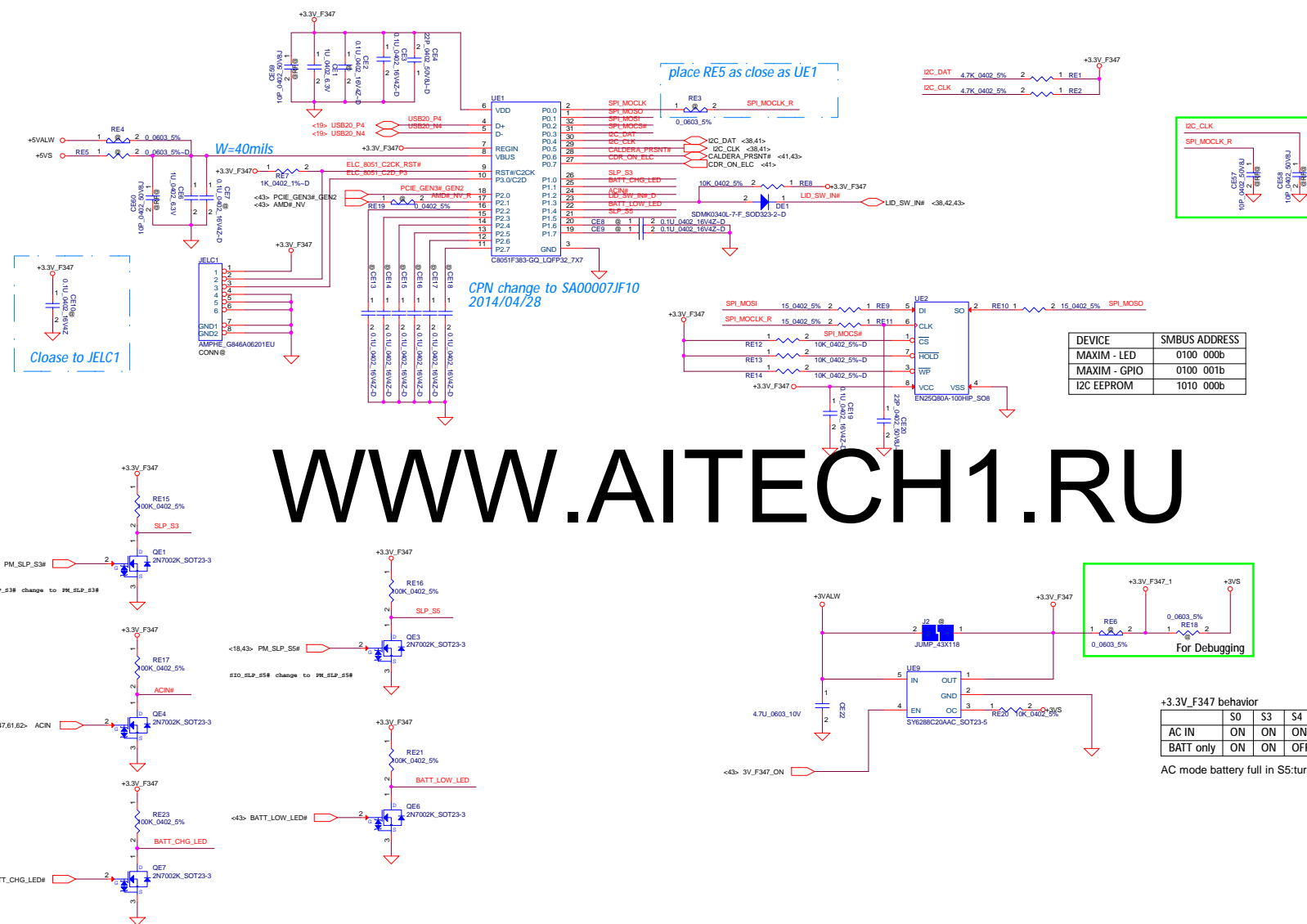


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				Rev. 0.1
				Sheet 36 of 78

CET DFT Confindinal



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## MAX7313 change to TI TLC59116F PWM expander

## Power LED

W=20mils

## Logic up LED board

## For IND/TP/HDD/PWR

## Power ON Circuit

## ON/OFF switch

ON/OFF switch power button  
Bottom Side pop only before MP

## For TouchPAD

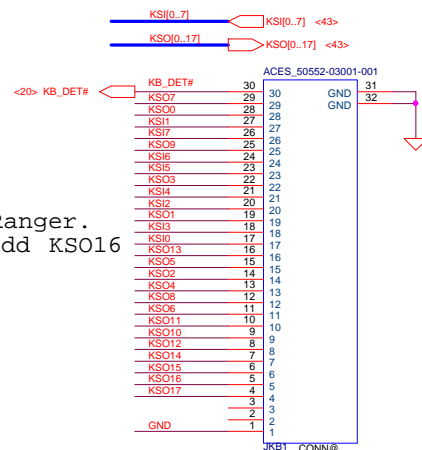
## Touchpad LED circuit

Change Symbol OK  
2/18 -Tarry

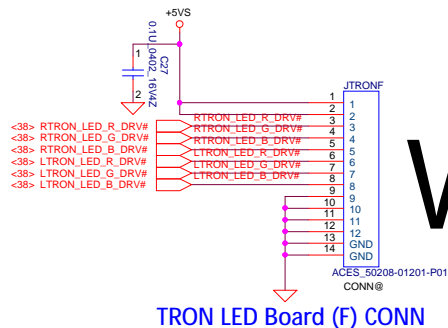
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Issued Date	2015/01/30	Deciphered Date	2016/12/31	Title	ELC (2)/TP/PWR SW
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				Checked	LA-C912P
				Date	Tuesday, July 21, 2015
				Sheet	38 of 78

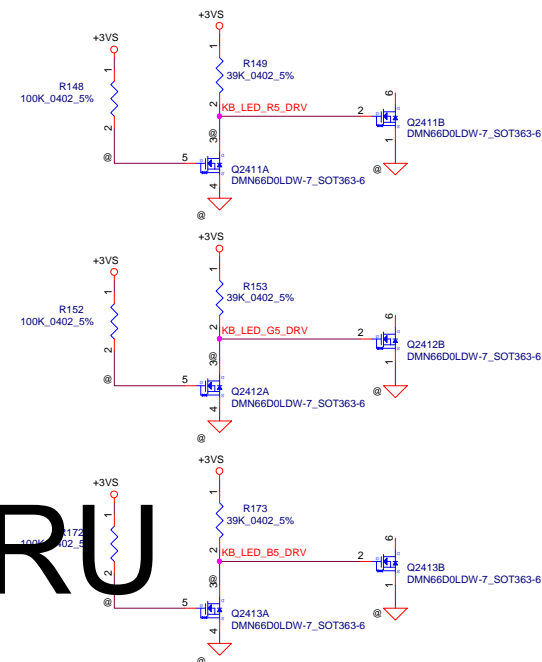
## INT\_KBD Conn.



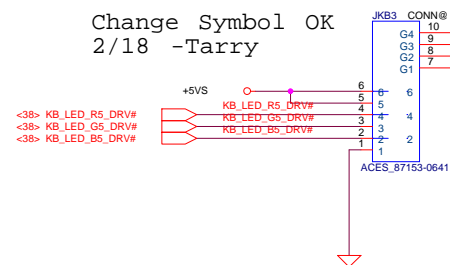
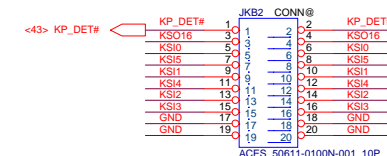
Net follow Ranger.  
Only Pin26 add KSO16



# WWW.AITECH1.RU

Hot Key Conn.  
PWM

Change Symbol OK  
2/18 -Tarry

Hot Key Conn.  
Key Pad

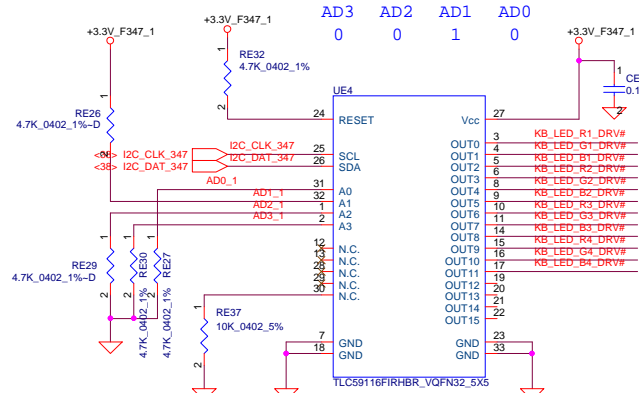
1/28 ADD

+5VS RE104 1 2 0.0603 5% +5V\_LED  
 +3VS RE105 1 2 0.0603 5%

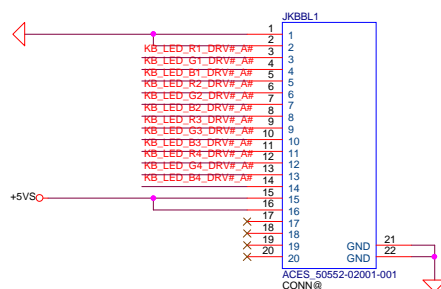
## K/B Backlight

AD3 AD2 AD1 AD0

0 0 1 0



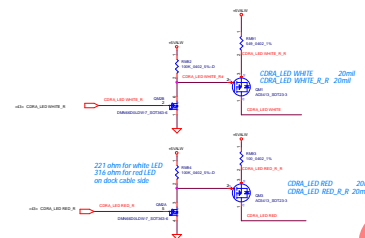
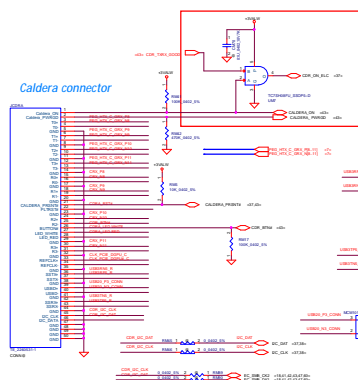
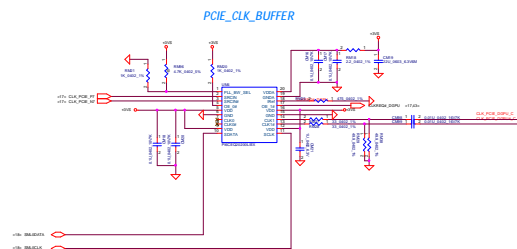
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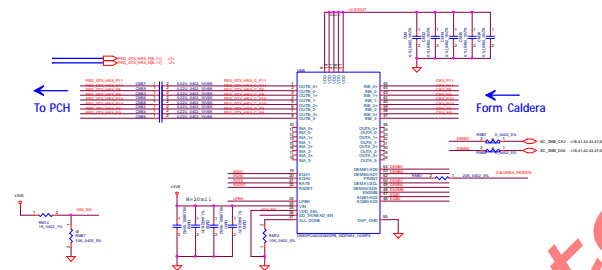
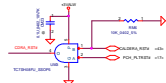
KB BL LED

Compal Electronics, Inc.			
Title		ELC(3)	
Size	Document Number	Rev	
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Date:	Tuesday, July 21, 2015	Sheet	40 of 78





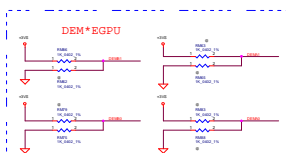
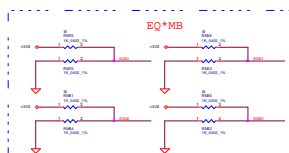
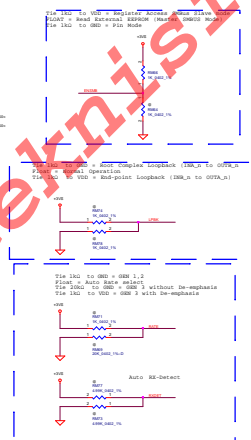
Follow ZAP00 design.



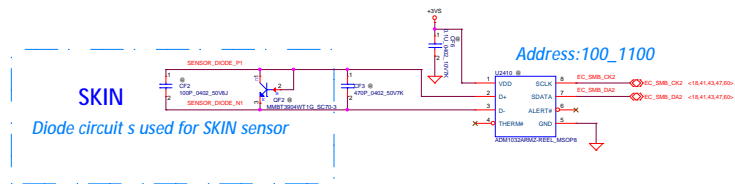
EQ Setting				
Filter	Low	High	dB of cut	Suggested Use
1	0	0	0	5 inch trace
2	0	0	-2	5 inch 50 oh trace
3	0	0	-4	5 inch 40 oh trace
4	0	0	-6	5 inch 30 oh trace
5	0	0	-8	10 inch 50 oh trace
6	0	0	-10	10 inch 40 oh trace
7	0	0	-12	12 inch 50 oh trace
8	0	0	-14	20 inch 40 oh trace
9	0	0	-16	25 to 30 inch 40 oh trace
10	0	0	-18	30 inch 40 oh trace
11	0	0	-20	35 inch 40 oh trace
12	0	0	-22	10m, 20m cable
13	0	0	-24	
14	0	0	-26	
15	0	0	-28	10m - 12 m cable
16	0	0	-30	
17	0	0	-32	
18	0	0	-34	
19	0	0	-36	
20	0	0	-38	
21	0	0	-40	
22	0	0	-42	
23	0	0	-44	
24	0	0	-46	
25	0	0	-48	
26	0	0	-50	
27	0	0	-52	
28	0	0	-54	
29	0	0	-56	
30	0	0	-58	
31	0	0	-60	

	DEMA	DEMA	DEMA	Suggested Use
Index	DEMA	DEMA	DEMA	
1	0	0	0	<5 inch - 4 - 48 inch
2	0	0	0	<5 inch - 4 - 48 inch
3	0	0	0	<5 inch - 4 - 48 inch
4	0	0	0	<5 inch - 4 - 48 inch
5	0	0	0	<5 inch - 4 - 48 inch
6	0	0	0	<5 inch - 4 - 48 inch
7	0	0	0	<5 inch - 4 - 48 inch
8	0	0	0	<5 inch - 4 - 48 inch
9	0	0	0	<5 inch - 4 - 48 inch
10	0	0	0	<5 inch - 4 - 48 inch
11	0	0	0	<5 inch - 4 - 48 inch
12	0	0	0	<5 inch - 4 - 48 inch
13	0	0	0	<5 inch - 4 - 48 inch
14	0	0	0	<5 inch - 4 - 48 inch
15	0	0	0	<5 inch - 4 - 48 inch
16	0	0	0	<5 inch - 4 - 48 inch

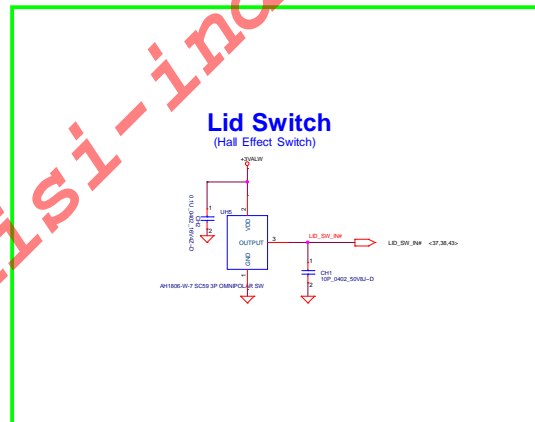
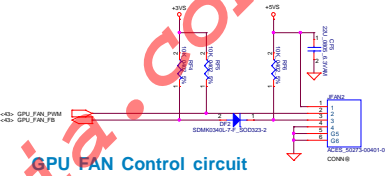
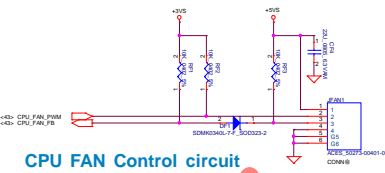
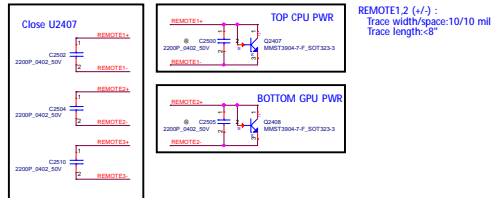
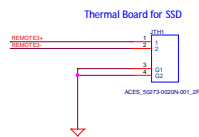
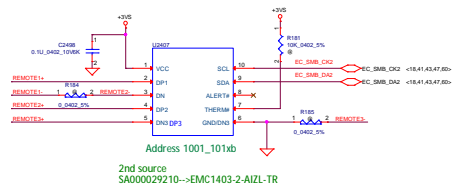
Level	Pin Setting	Description	Value	Unit
1	0	Low to High	5	ms
2	1	High to Low	5	ms
3	2	Float	10	ms
4	3	Low to High	5	ms



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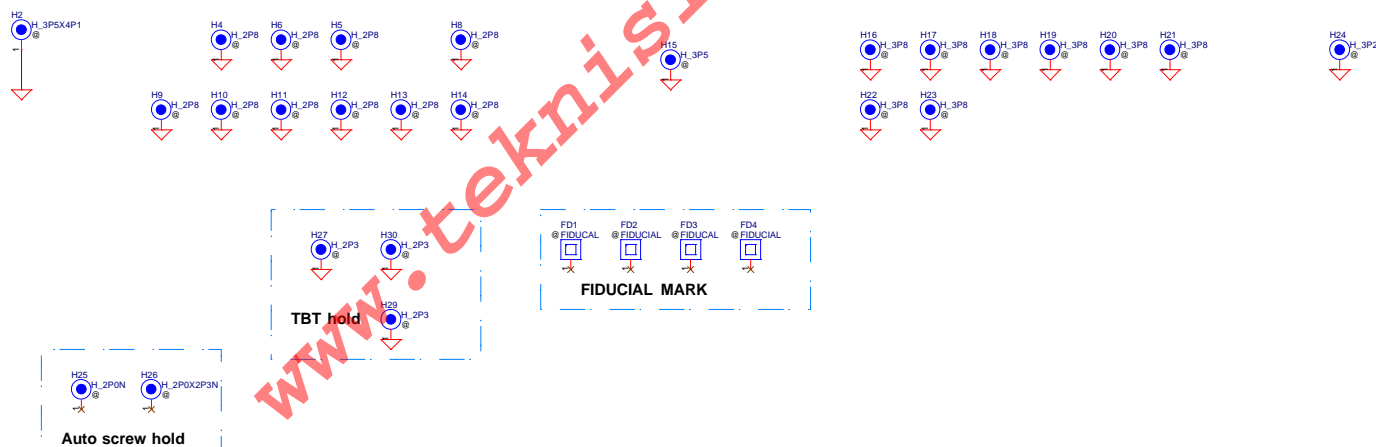
Fintek thermal sensor-&gt; CPU core, DIMM



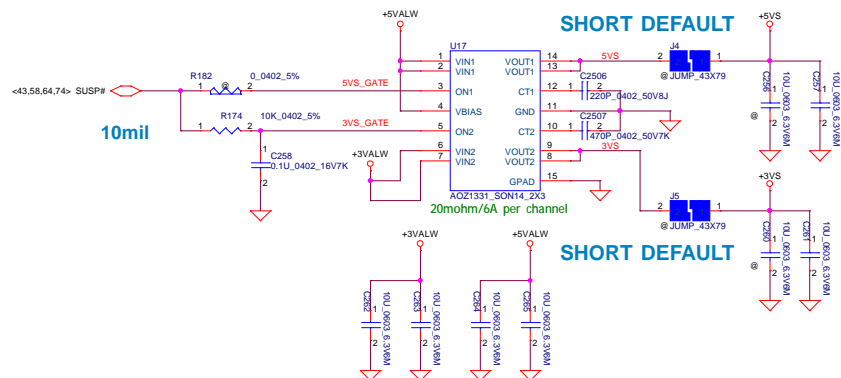
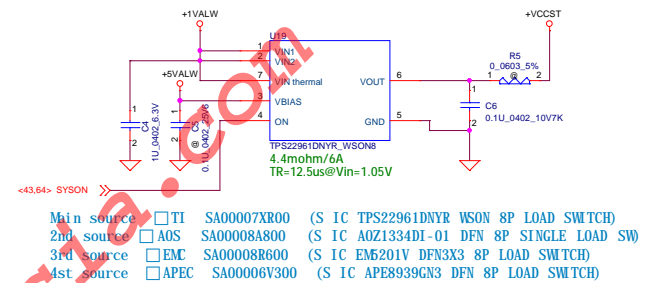
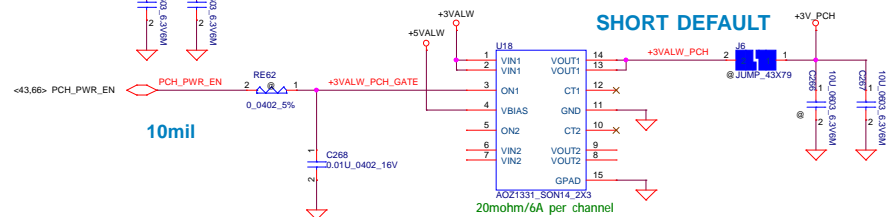
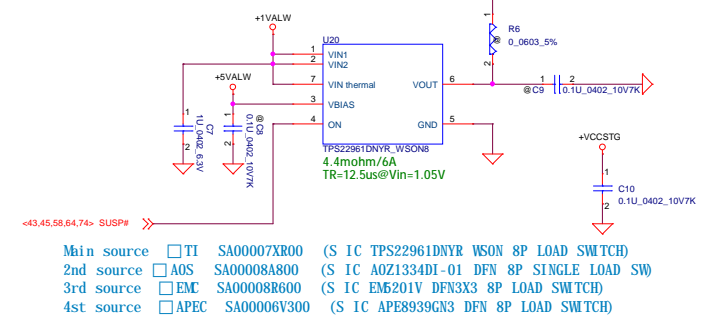
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LA-C911P		Rev
Date		Rev
2015/01/30		Rev
2015/01/30		Rev



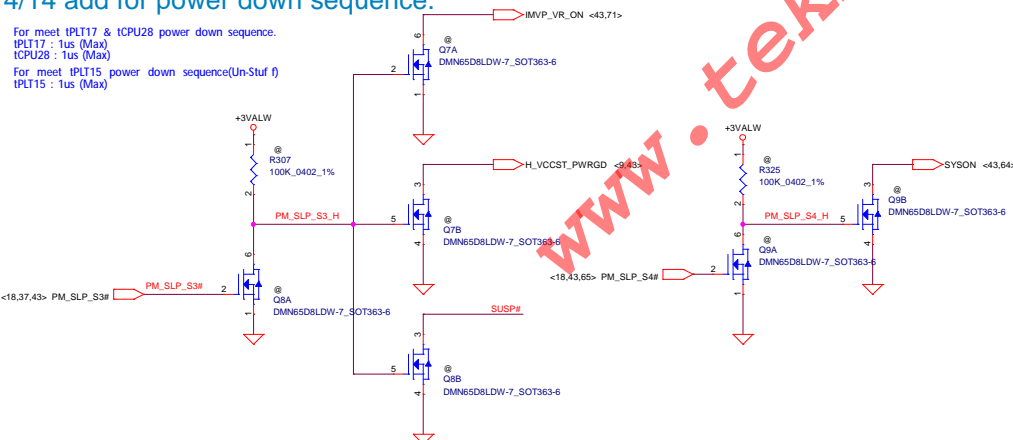
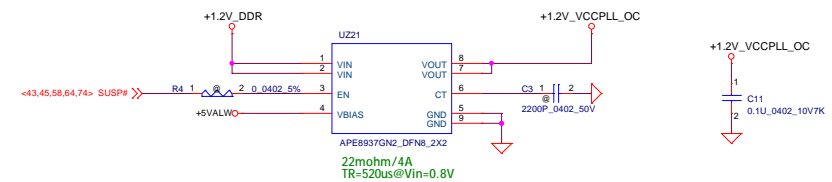
## Screw Hole



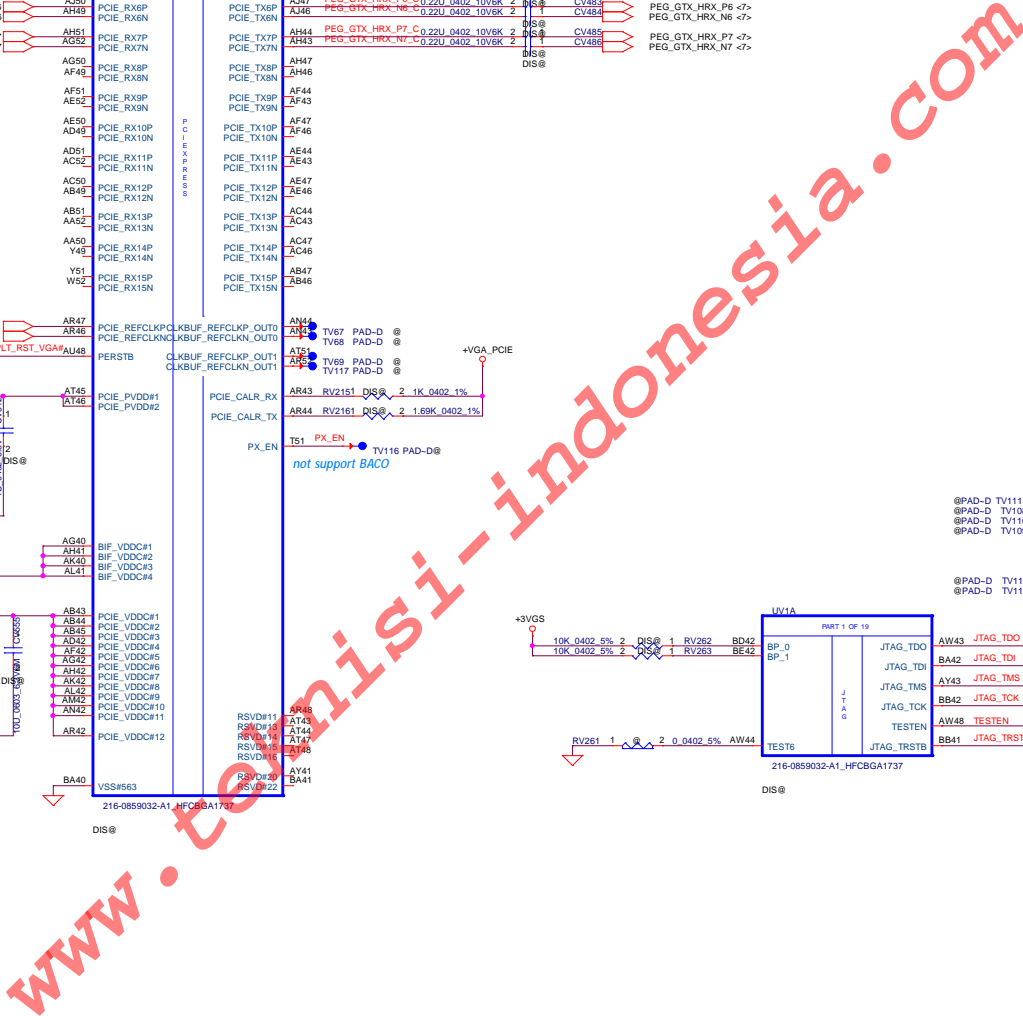
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				Size	Document Number
				LA-C911P	
Date: Tuesday, July 21, 2015				Sheet	44 of 78
				Rev	0.1

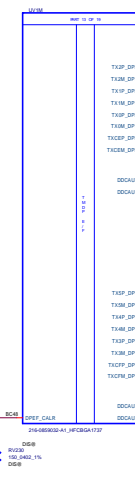
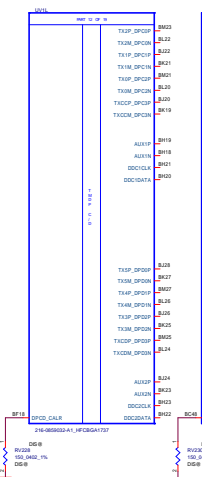
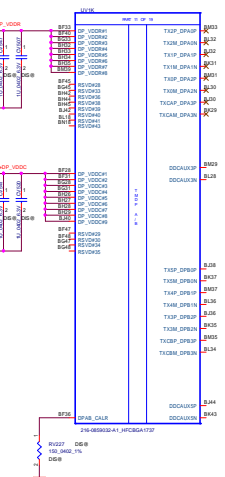
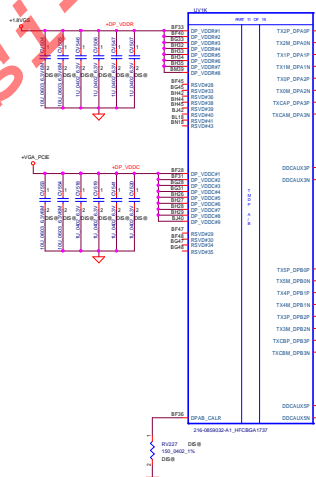
**+5VS and +3VS switch****+VCCST Load Switch****+3VALW\_PCH switch****+VCCSTG source****4/14 add for power down sequence.**

For meet IPLT17 & ICPU28 power down sequence.  
IPLT17 : 1us (Max)  
ICPU28 : 1us (Max)  
For meet IPLT15 power down sequence(Un-Stuf f)  
IPLT15 : 1us (Max)

**+1.2V\_VCCPLL\_OC**

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				Size	Rev
				Document Number	0.1
				LA-C912P	
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CET DFT Confindinal



Timing diagram for the 4750 device. The diagram shows a square wave for '4750\_S402\_1%' and a signal for 'DS68C03A'. Below the diagram are two tables.

C [nF]	Bits(5:4)
680	00
82	01
10	10
NC	11

R_pos	R_pd	Bits (3:1)	VRAM
NC	4750	000	Hynix H59C404M/R-T2C
8450	2000	001	
4510	2000	010	
6980	4990	011	
4510	4990	100	
3240	5620	101	
3400	10000	110	
4750	NC	111	Samsung K404132BF-HC08

R_po	R_pd	Bits [3:1]	VRAM
800	4750	000	Hynix H5GC4H24MFR-T2C
8450	2000	001	
4530	2000	010	
6980	4990	011	
4530	4990	100	
3240	5620	101	
3400	10000	110	
4750	800	111	
			Samsung K4G41325FC-HC03

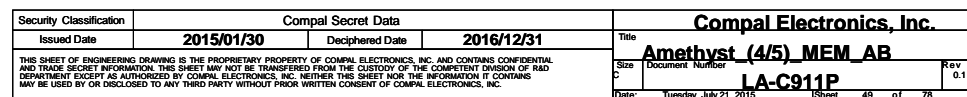
Security Classification		Compul Secret Data		<b>Compul Electronics, Inc.</b> <b>Amethyst (2/5) GPIO/MSIC</b>	
Issued Date		2015/01/30	Declassified Date	2016/12/31	Title Document Number <b>LA-C9181</b>
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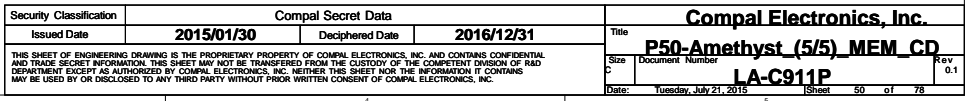




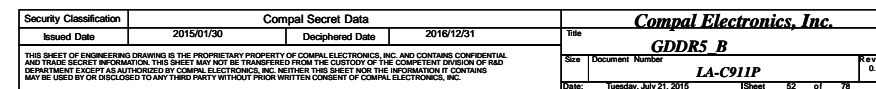
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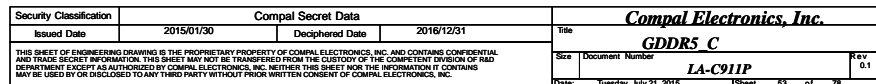


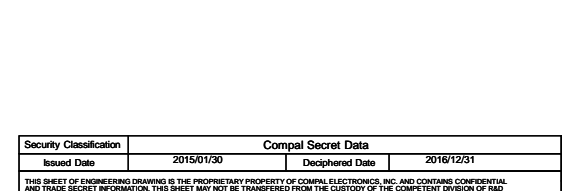
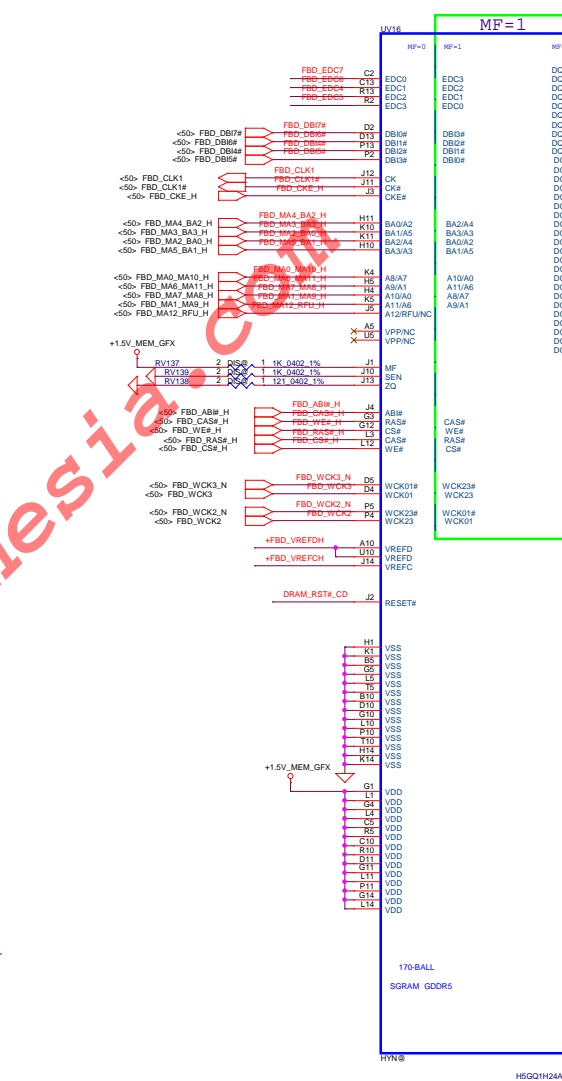
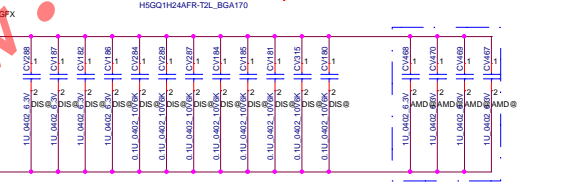
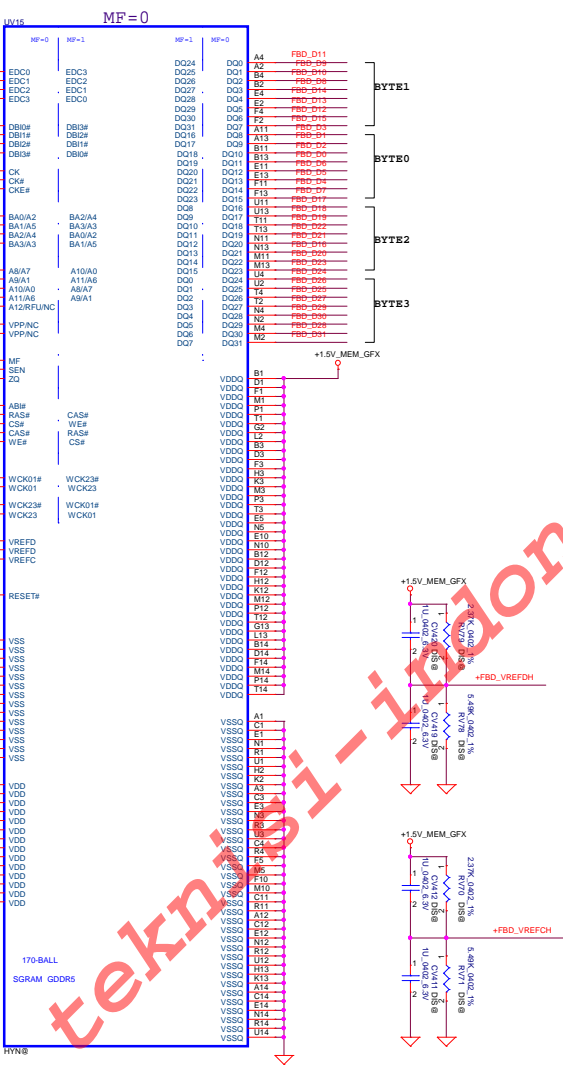
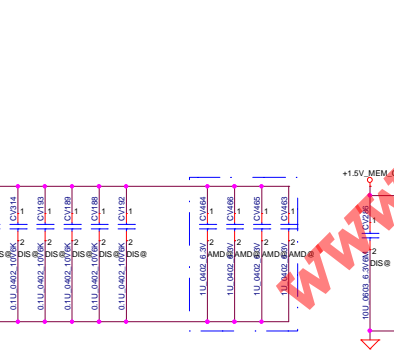
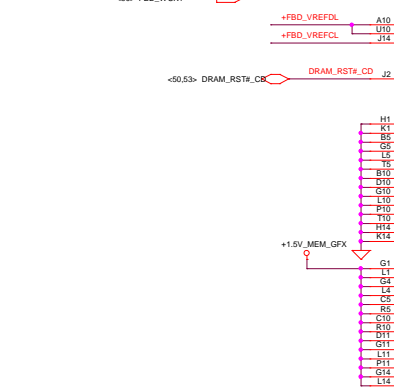
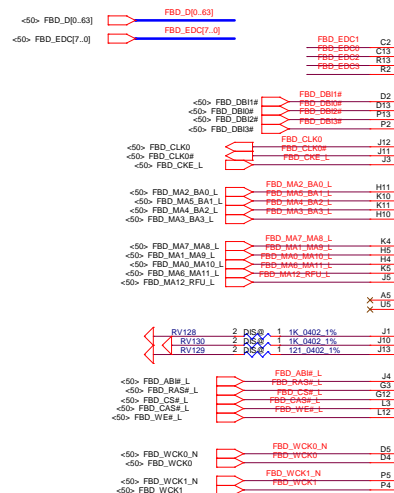


$$MF = 0$$
CET DFT Confindinal



## MF=1



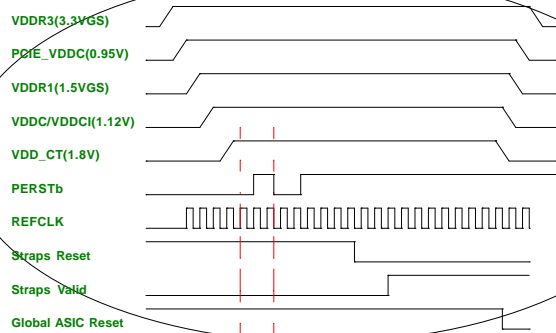


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				Date Issued	July 21, 2015
				Page	54 of 78

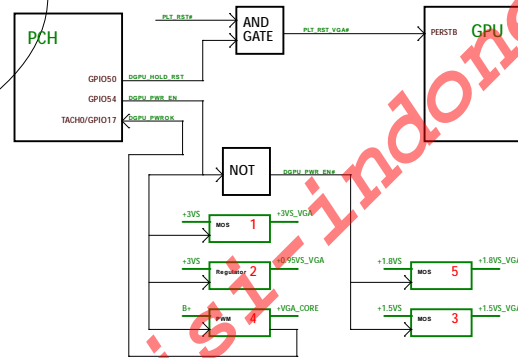


## Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ $\mu$ s.
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.
3. VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
4. For power down, reversing the ramp-up sequence is recommended.



CPU part



+VGA_CORE(NV VDD)	10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)
VDDCI	3.5A	1	3
+VDDGFX			

+VGA_PCIE	10uF	1uF	0.1uF
PCI_E_VDDC	2.5A	2 (1@)	5 (1@)
BIF_VDDC	1.4A	0	0
SPLL_VDDC	100mA	1	1

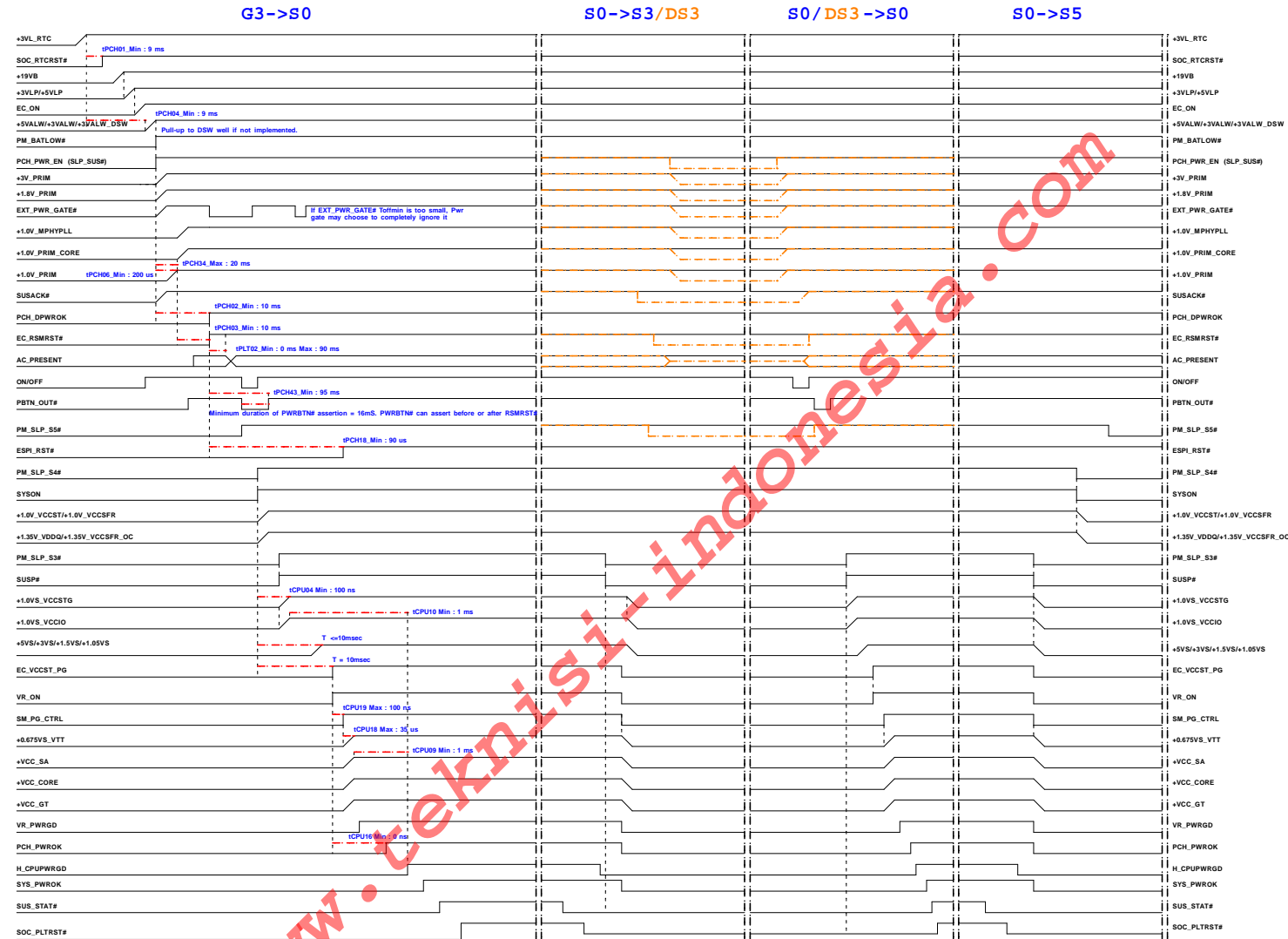
+1.35V_MEM_LFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1	1.5A	3	5	5

+1.8VGS	10uF	1uF	0.1uF
PCI_E_PVDD	100mA	1	1
MPLL_PVDD	130mA	1	1
SPLL_PVDD	75mA	1	1
VDDR4	(300mA)	0	0
VDD_CT	13mA	1	1
+TSVDD	13mA	1	1
+DP_VDDR	0	0	0
+DP_VDDC	0	0	0

+3VGS	10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)

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LA-C911P				Rev. 1.1
Date: 2015/01/30				Sheet: 35 of 39

[AAX06-PWR Sequence\_SKL-H 4+4\_DDR4\_Volume\_NON CS]



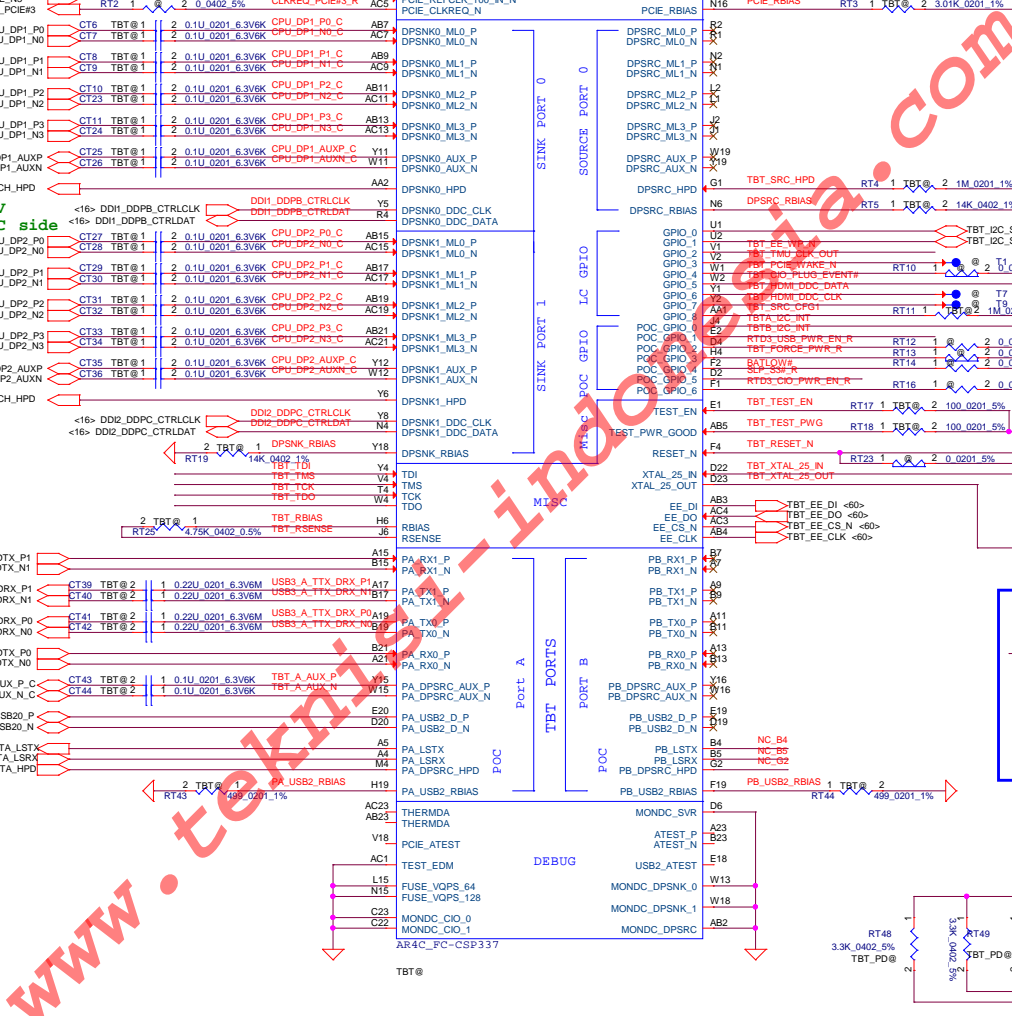
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Issued Date	2015/07/09	Dispersed Date	
Title			
Power Sequence			
Doc No.	Doc Name	Doc Number	Doc Date
LA-CHUP			
Version	Version	Rev	Rev
1.0	1.0	1.0	1.0



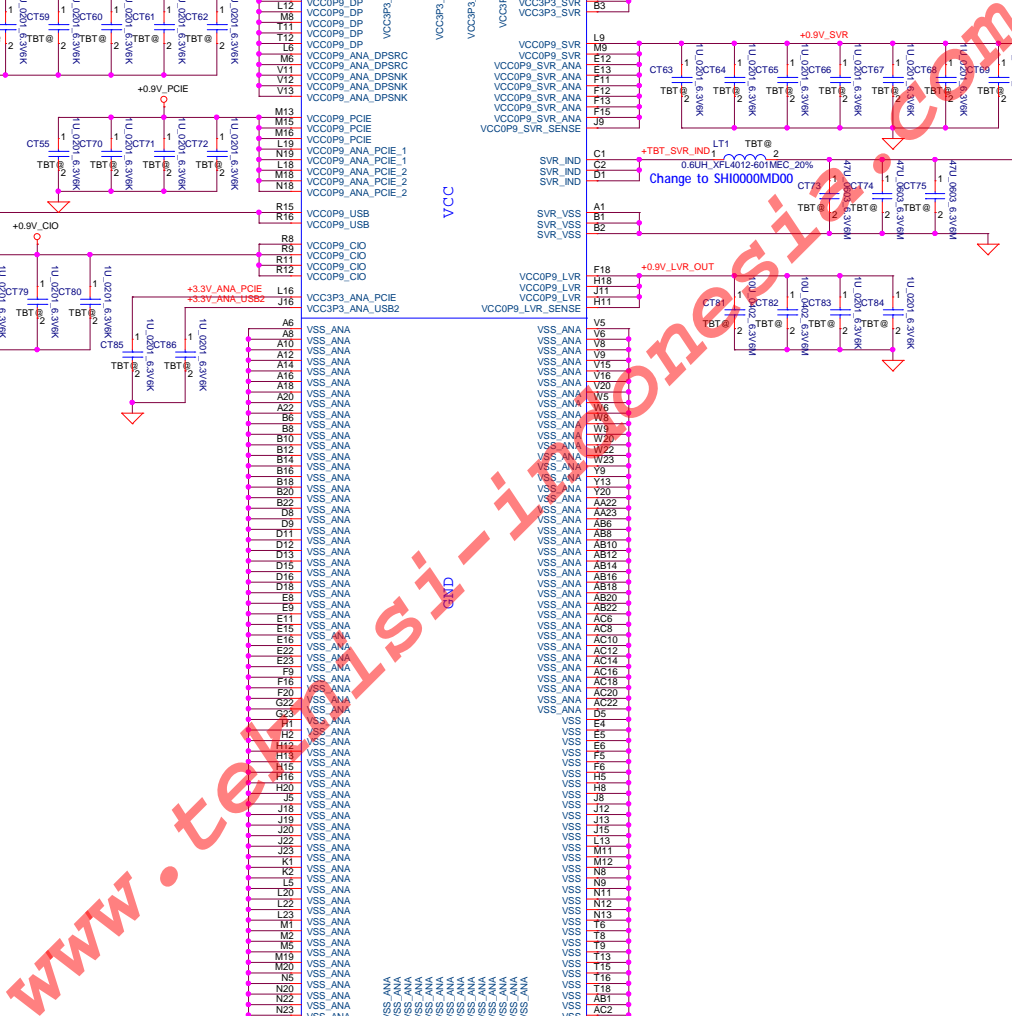
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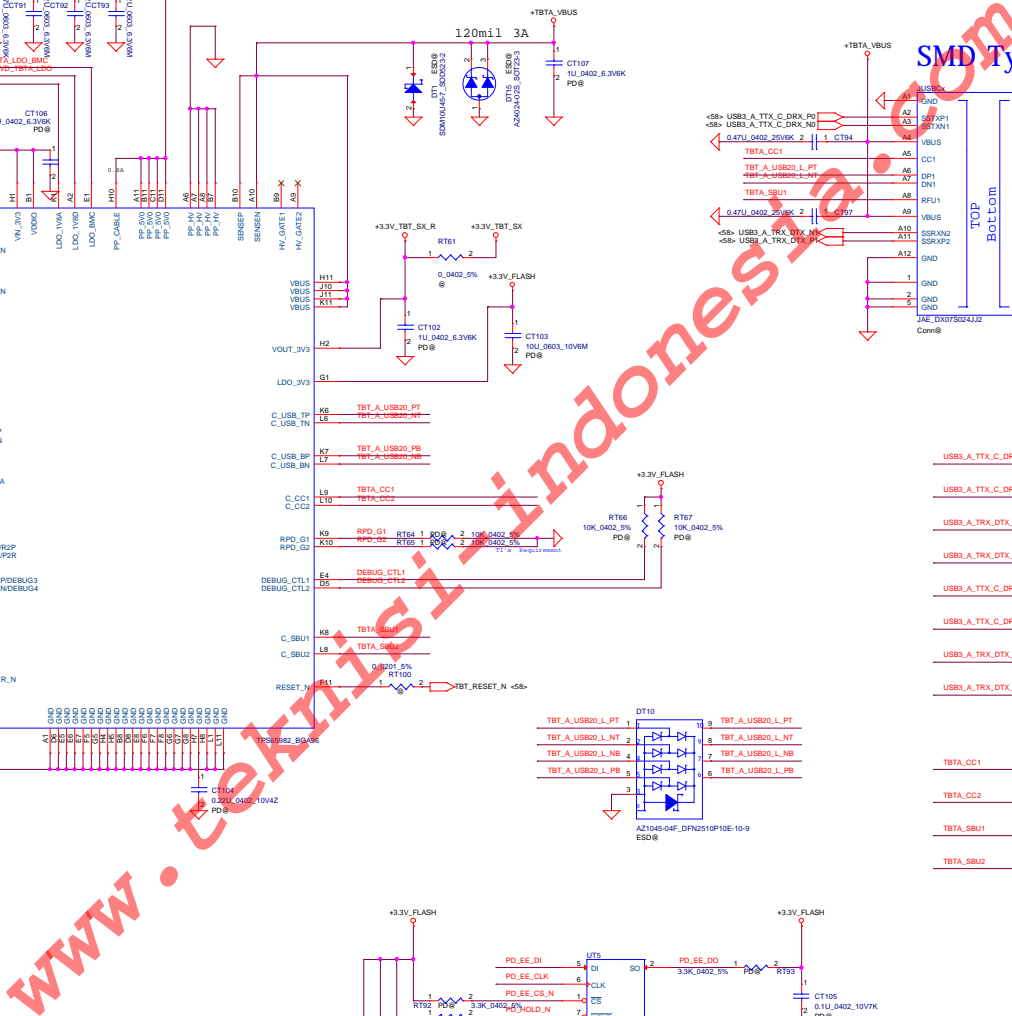
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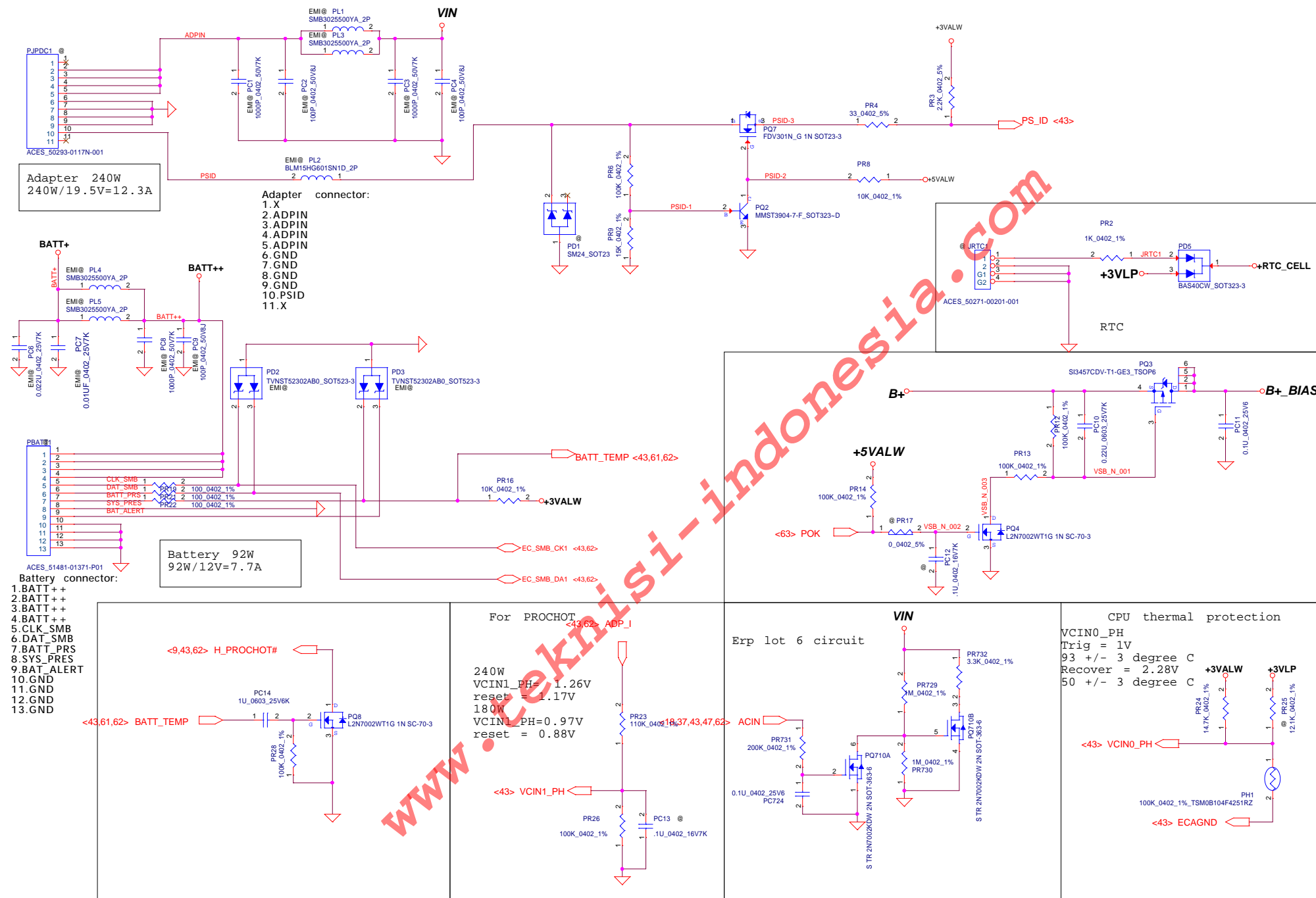
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				Date:	Wednesday, July 22, 2015	Sheet 58 of 78



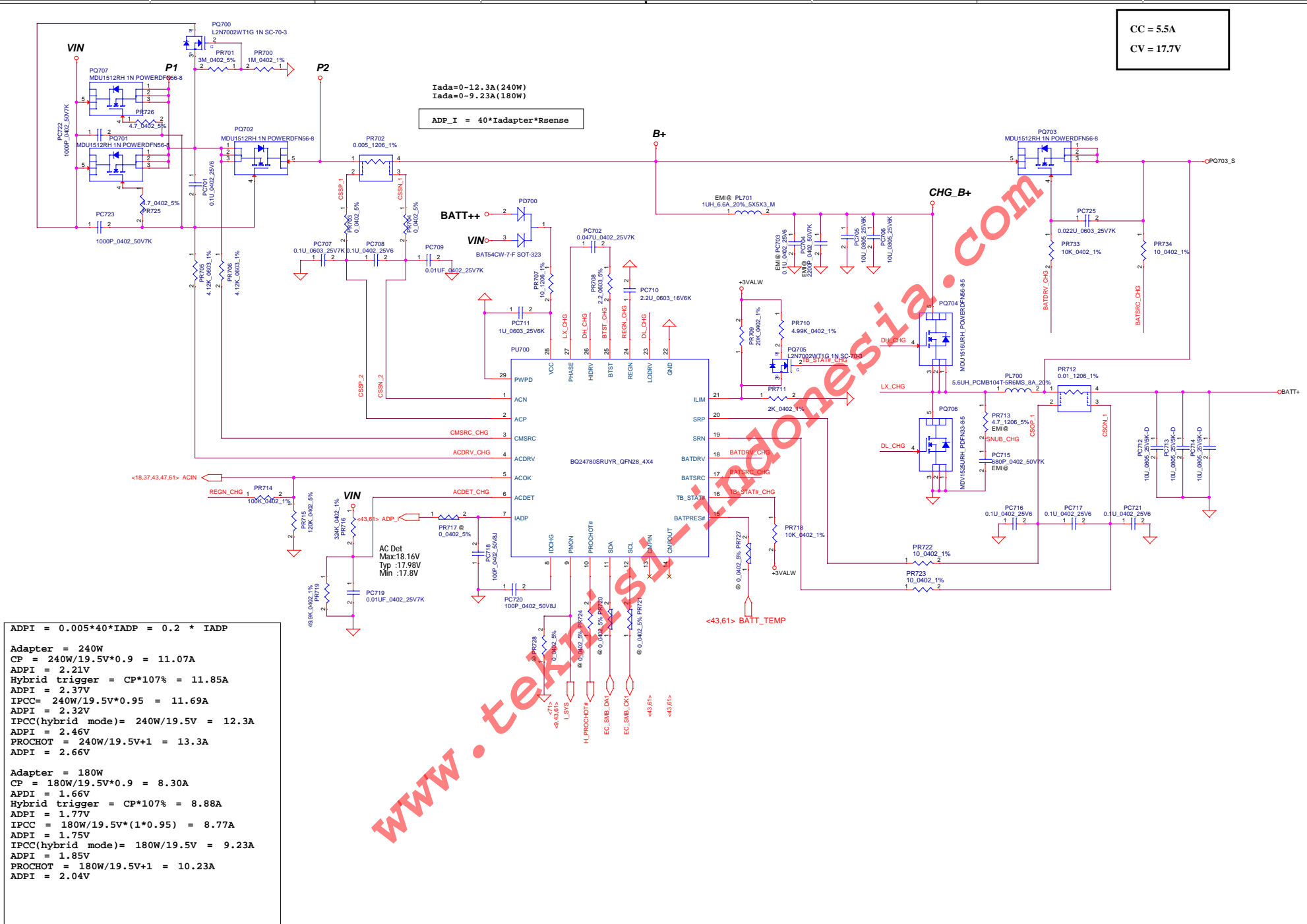
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			Rev	0.1

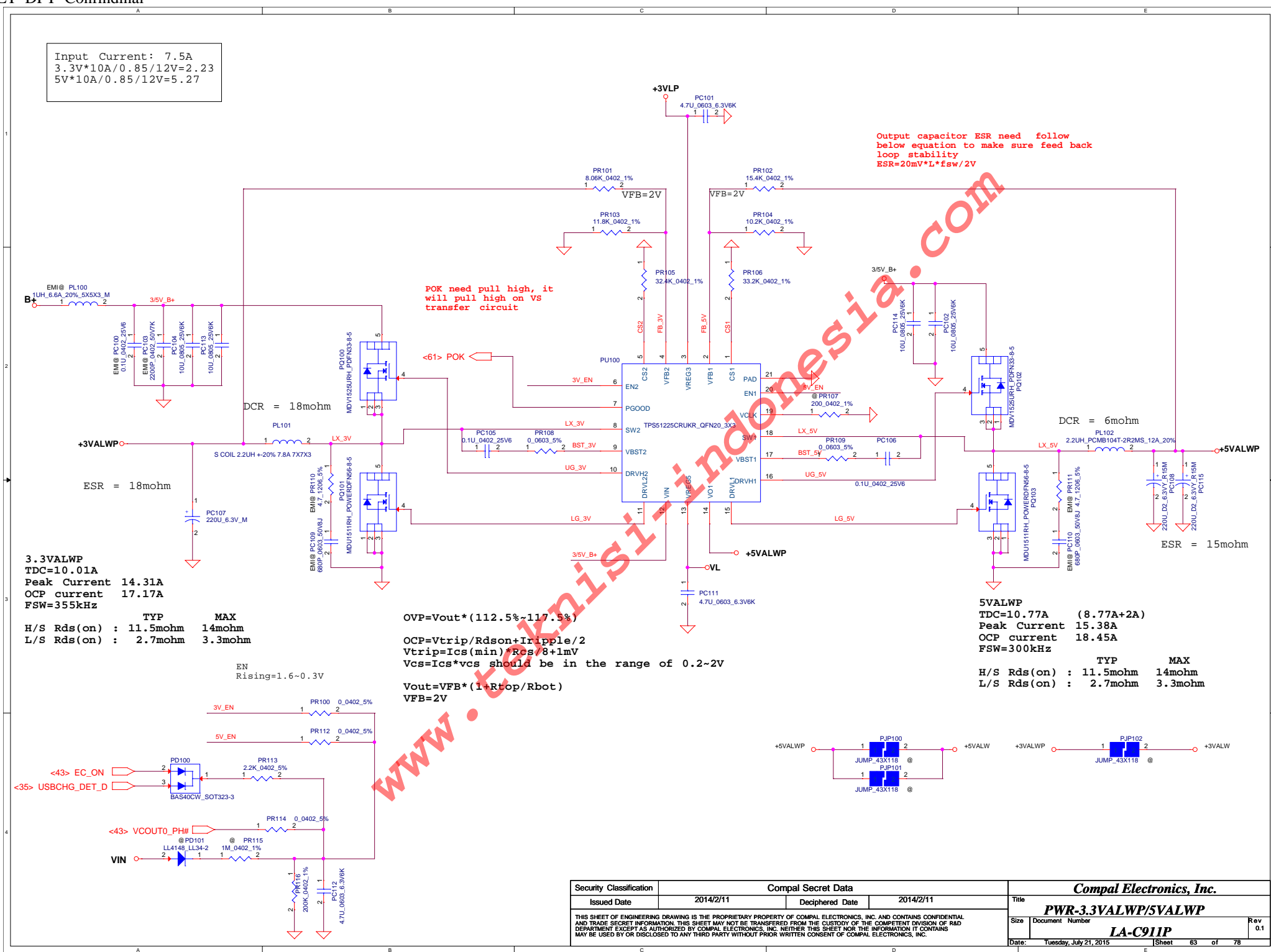


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				LA-C912P	
				Date:	Tuesday, July 21, 2015
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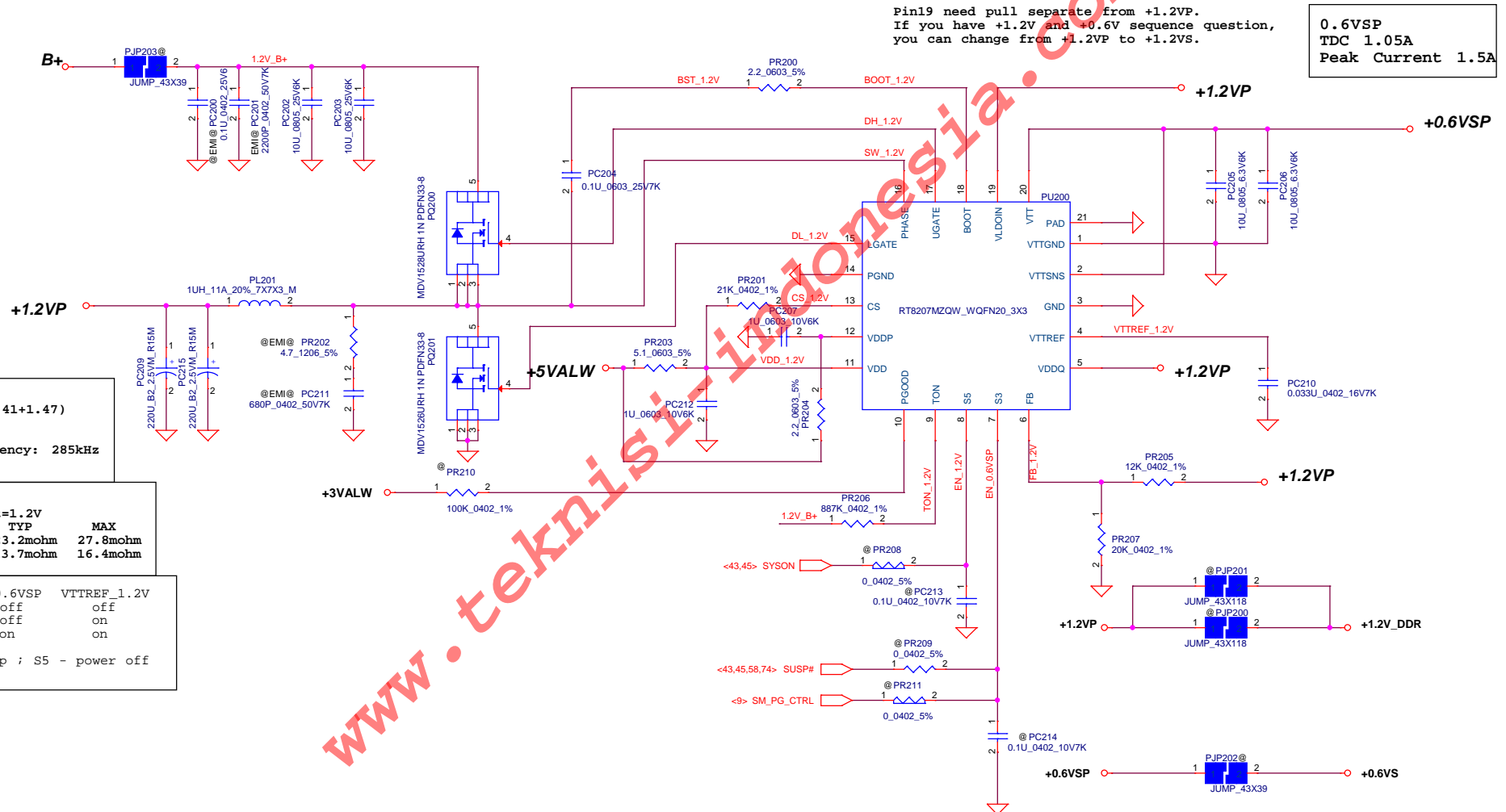


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Input Current: 7.5A  
 $3.3V \cdot 10A / 0.85 / 12V = 2.23$   
 $5V \cdot 10A / 0.85 / 12V = 5.27$



Input Current: 1A  
 $1.2V \cdot 8.88A / 0.85 / 12V = 1$



1.2VP  
TDC=8.88A (7.41+1.47)  
Ipeak=12.68A  
OCP=15.21A  
Switching Frequency: 285kHz

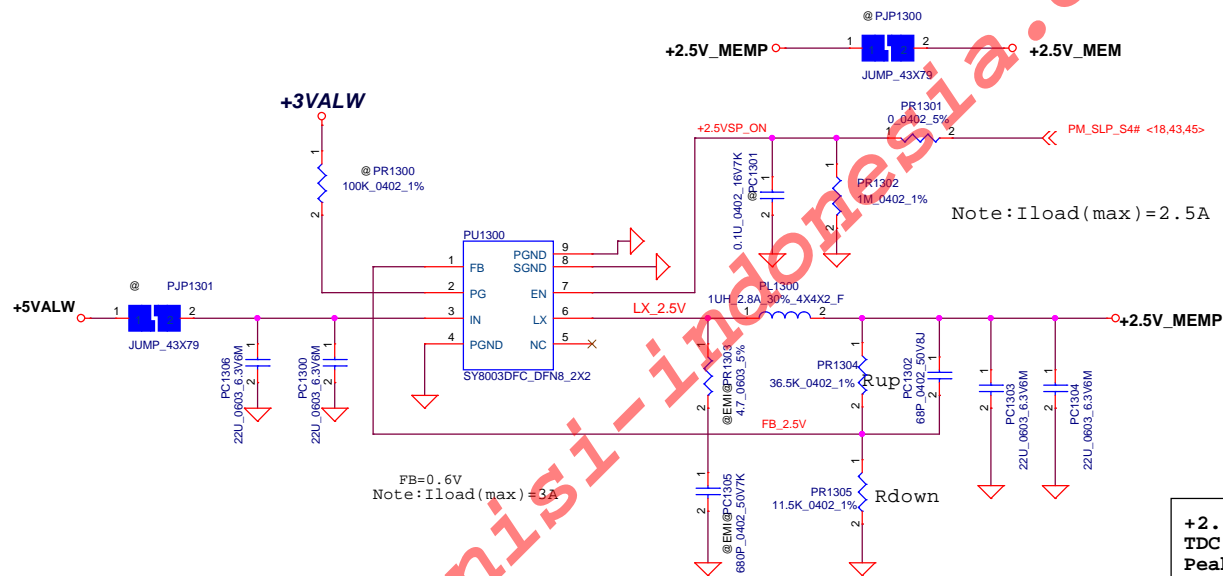
OVP: 110%~120%		
VFB=0.75V, Vout=1.2V		
	TYP	MAX
H/S Rds(on) :	23.2mohm	27.8mohm
L/S Rds(on) :	13.7mohm	16.4mohm

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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				<b>LA-C911P</b> Date: Tuesday, July 21, 2015 Sheet 64 of 78	
				Rev	0.1



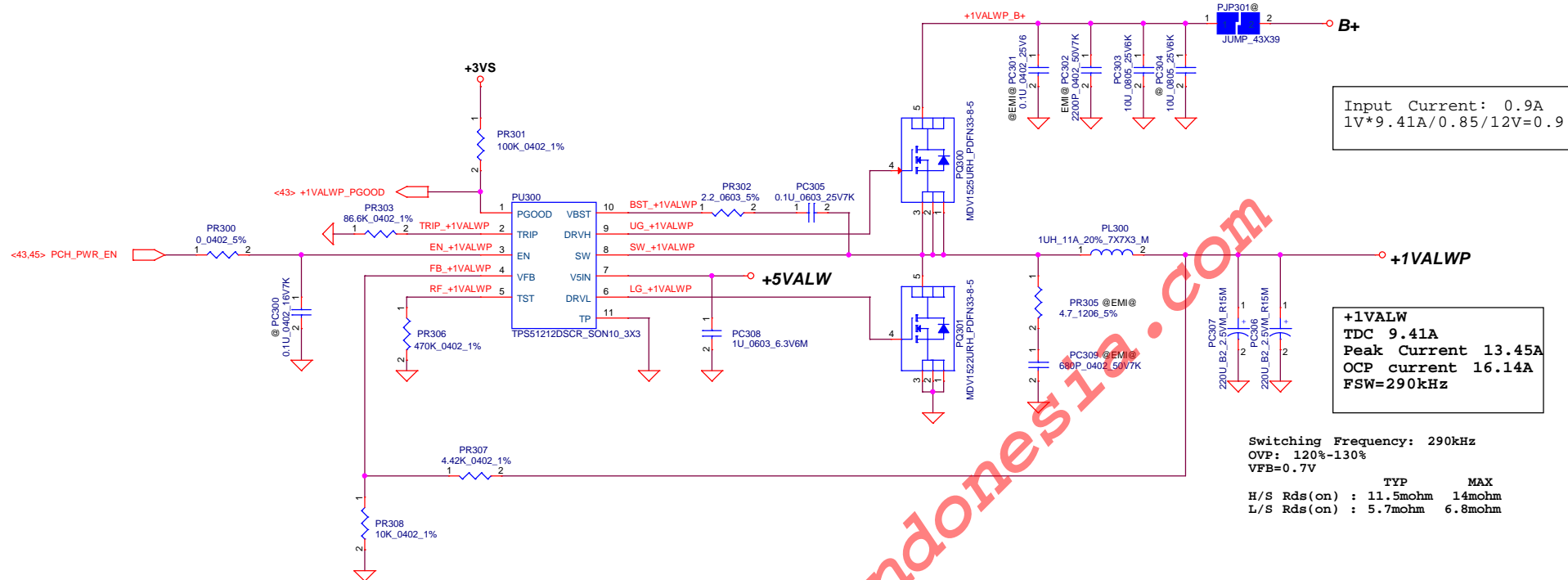


Note:  
When design  $V_{in}=5V$ , please stuff snubber  
to prevent  $V_{in}$  damage

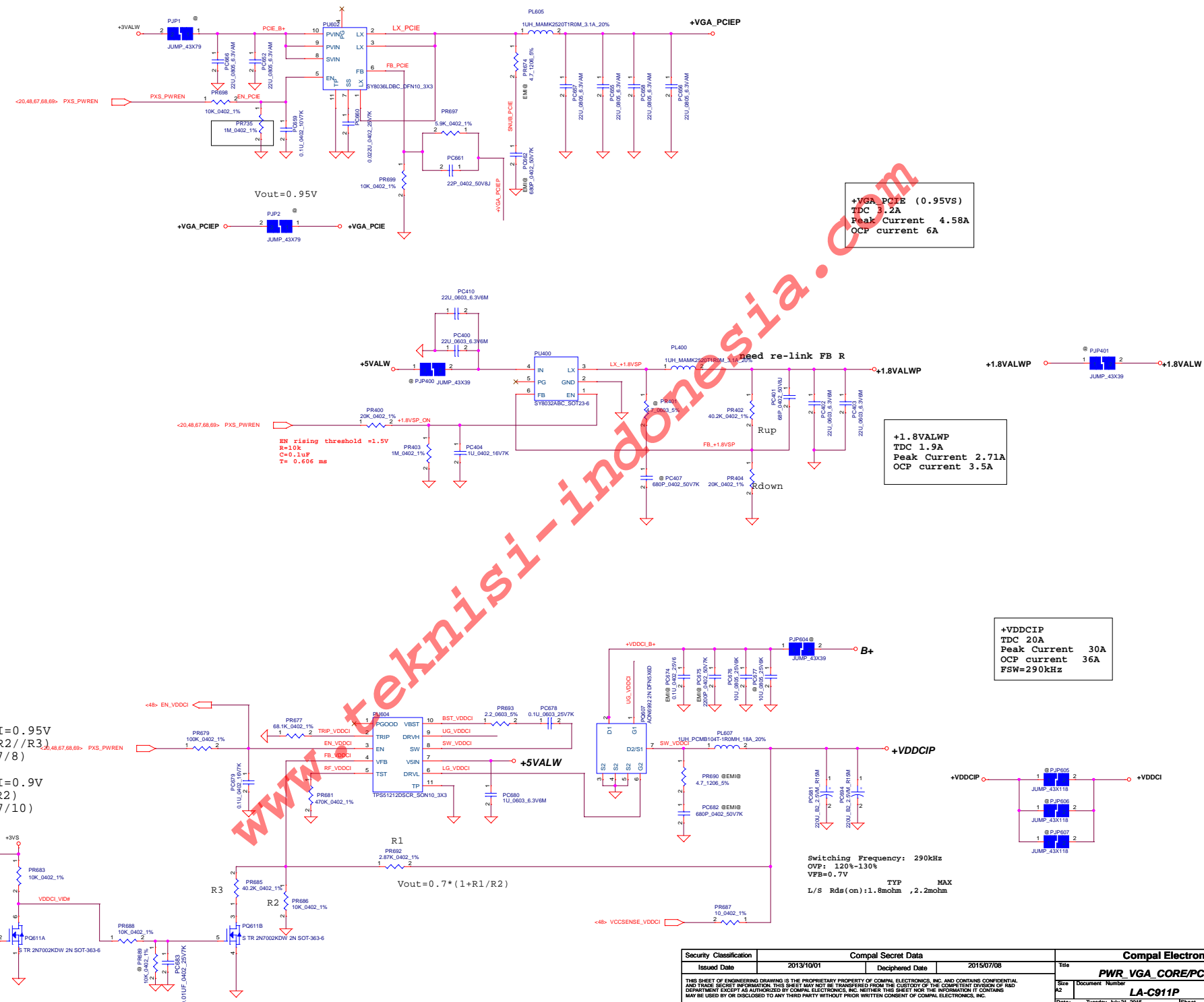
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

```
+2.5V_MEM
TDC 0.63A
Peak Current 0.9A
OCP Current 3.5A
```

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				Size	Documnet Number	Rev
				<b>LA-C911P</b>		
Date: Tuesday, July 21, 2015				Sheet	65	of 78

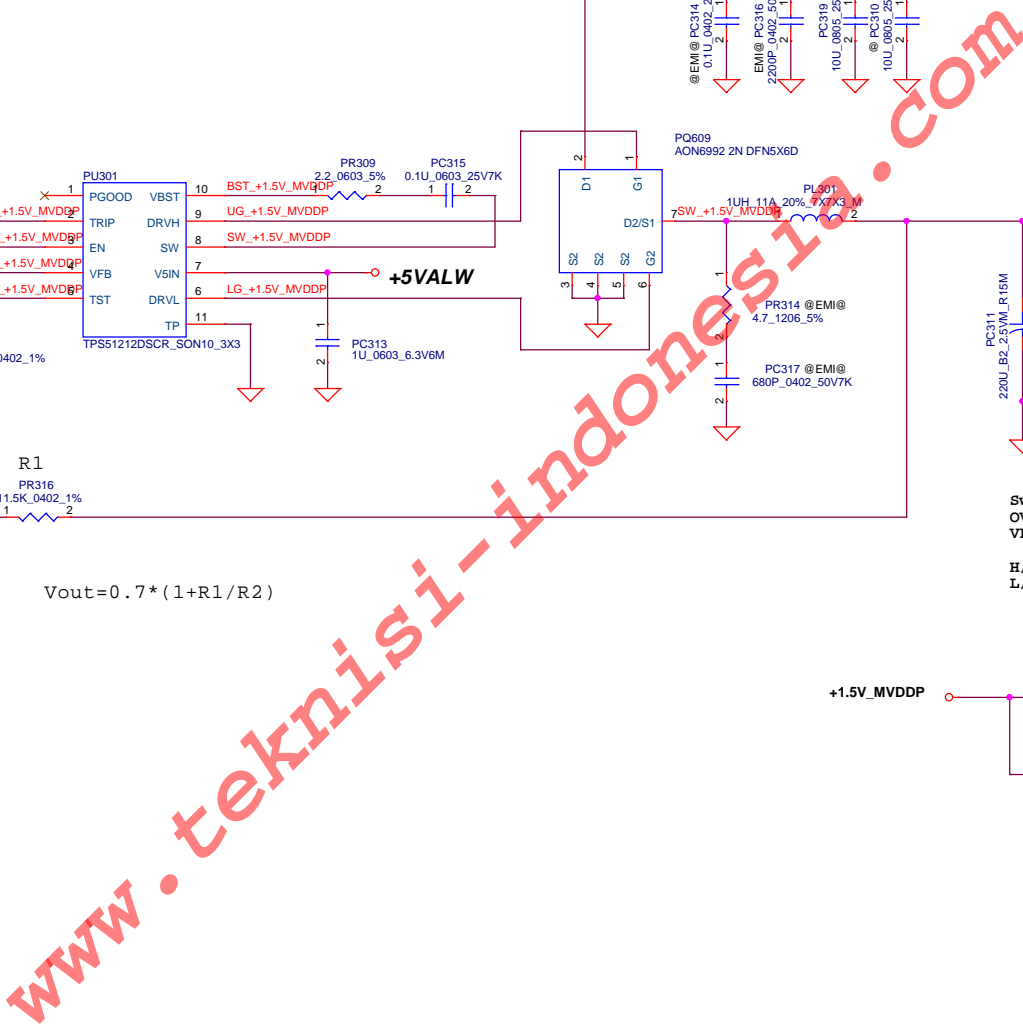


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				Sheet	66 of 78




Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/10/01	Deciphered Date	2015/07/08	Title	
				PWR_VGA_CORE/PCIE	
				Size	Document Number
				A2	LA-C911P
				Date	Tuesday, July 21, 2015
				Sheet	67 of 78
				Rev	0.1

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				<b>LA-C911P</b>	
				Date: <b>Thursday, April 23, 2015</b>	
				Sheet: <b>05</b> of <b>78</b>	

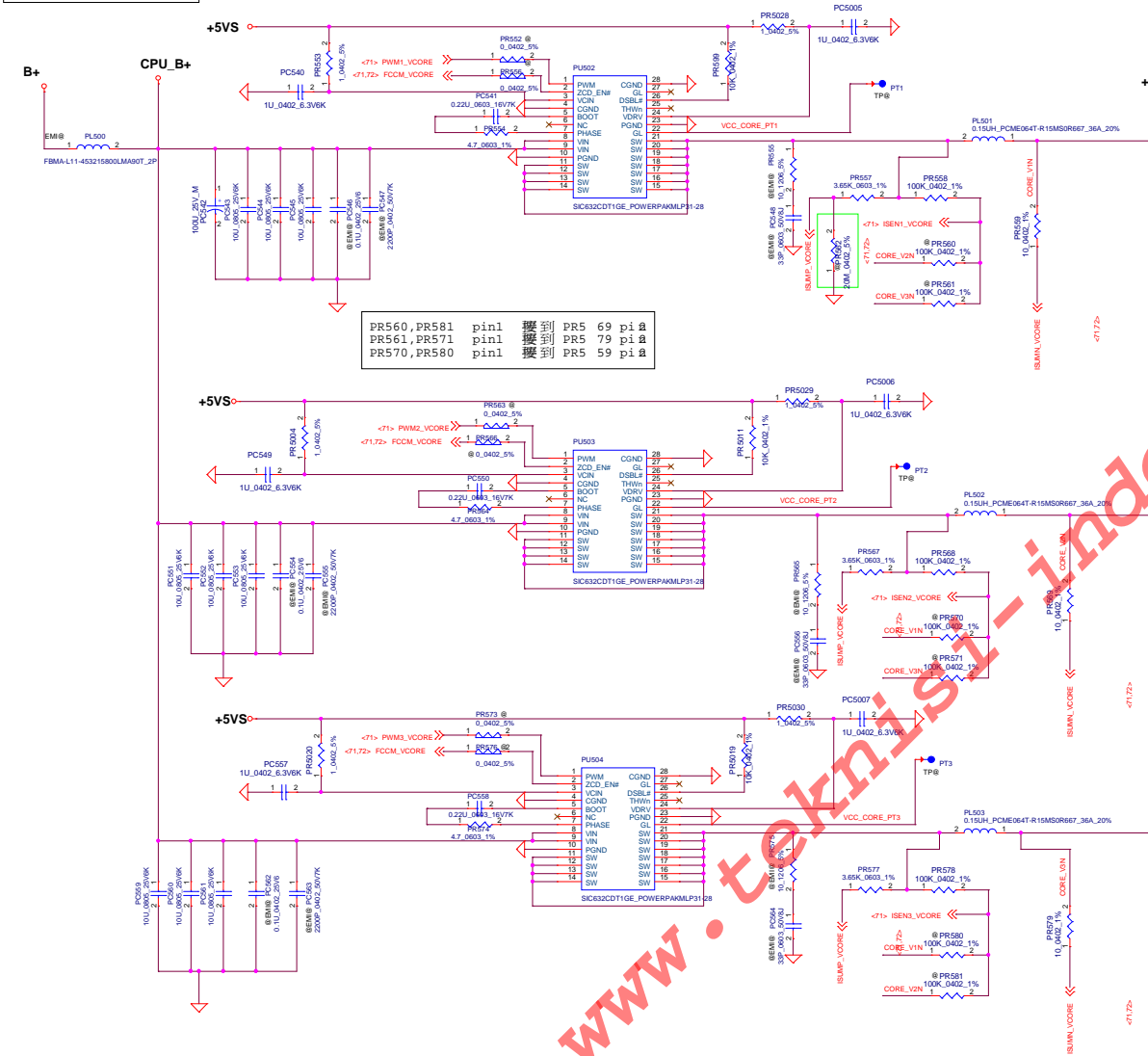


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	<b>Compal Electronics, Inc.</b>		
	<b>PWR VCORE ISL95855</b>		
	<b>LA-C912P</b>		
	Date: <b>Tuesday, July 21, 2015</b>	Sheet: <b>71</b>	of: <b>78</b>

VCC\_CORE  
TDC PL2 :56A  
Peak Current 68A  
OCP Current 81.6A  
DCR 0.66mohm +/-7%  
Load Line 1.8mV/A



PR560,PR581	pin1	婆到	PR5	69	pi a
PR561,PR571	pin1	婆到	PR5	79	pi a
PR570,PR580	pin1	婆到	PR5	59	pi a



**Compal Electronics, Inc.**

**PWR\_VCORE\_VCORE**

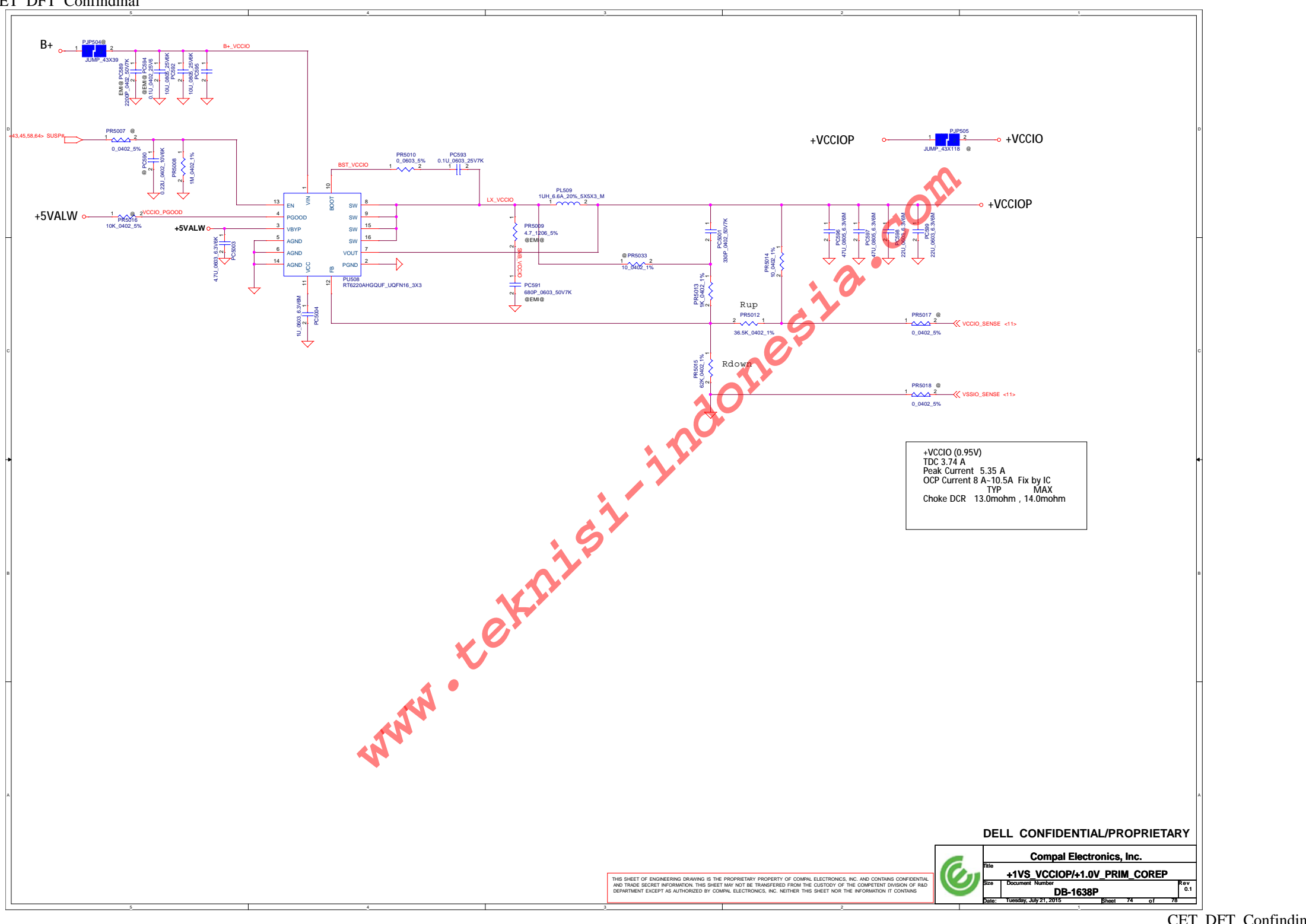
**LA-C912P**

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+VCCIO (0.95V)  
TDC 3.74 A  
Peak Current 5.35 A  
OCP Current 8 A-10.5A Fix by IC  
TYP MAX  
Choke DCR 13.0mohm , 14.0mohm



<b>Compal Electronics, Inc.</b>			
Title	<b>+1VS VCCIOP/+1.0V PRIM COREP</b>		
Size	Document Number	<b>DB-1638P</b>	Rev 0.1
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+VCC\_CORE

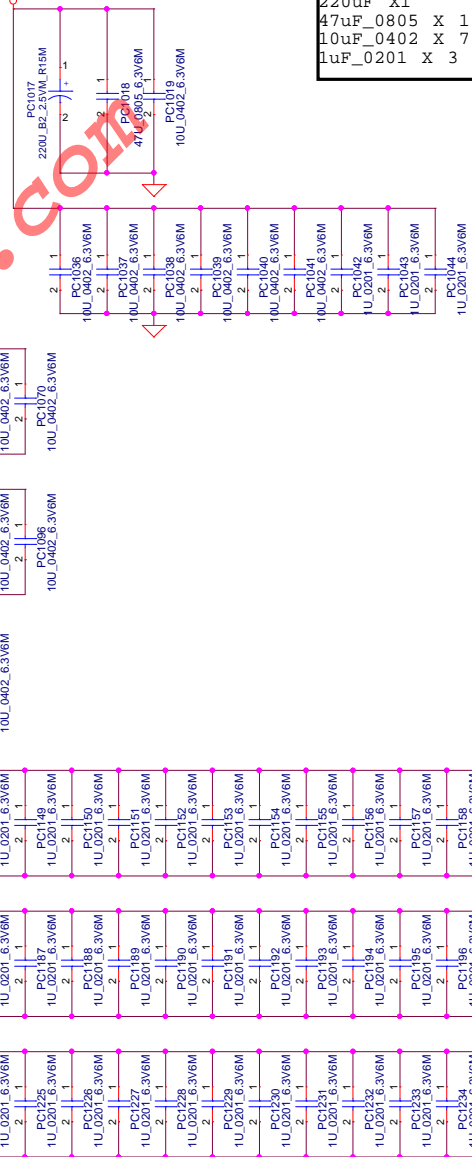


VCC\_CORE  
220uF X3  
47uF\_0805 X 4  
22uF\_0603 X 8  
10uF\_0402 X 28  
1uF\_0201 X 63

+VCCGT



+VCCSA



VCC\_SA  
220uF X1  
47uF\_0805 X 1  
10uF\_0402 X 7  
1uF\_0201 X 3

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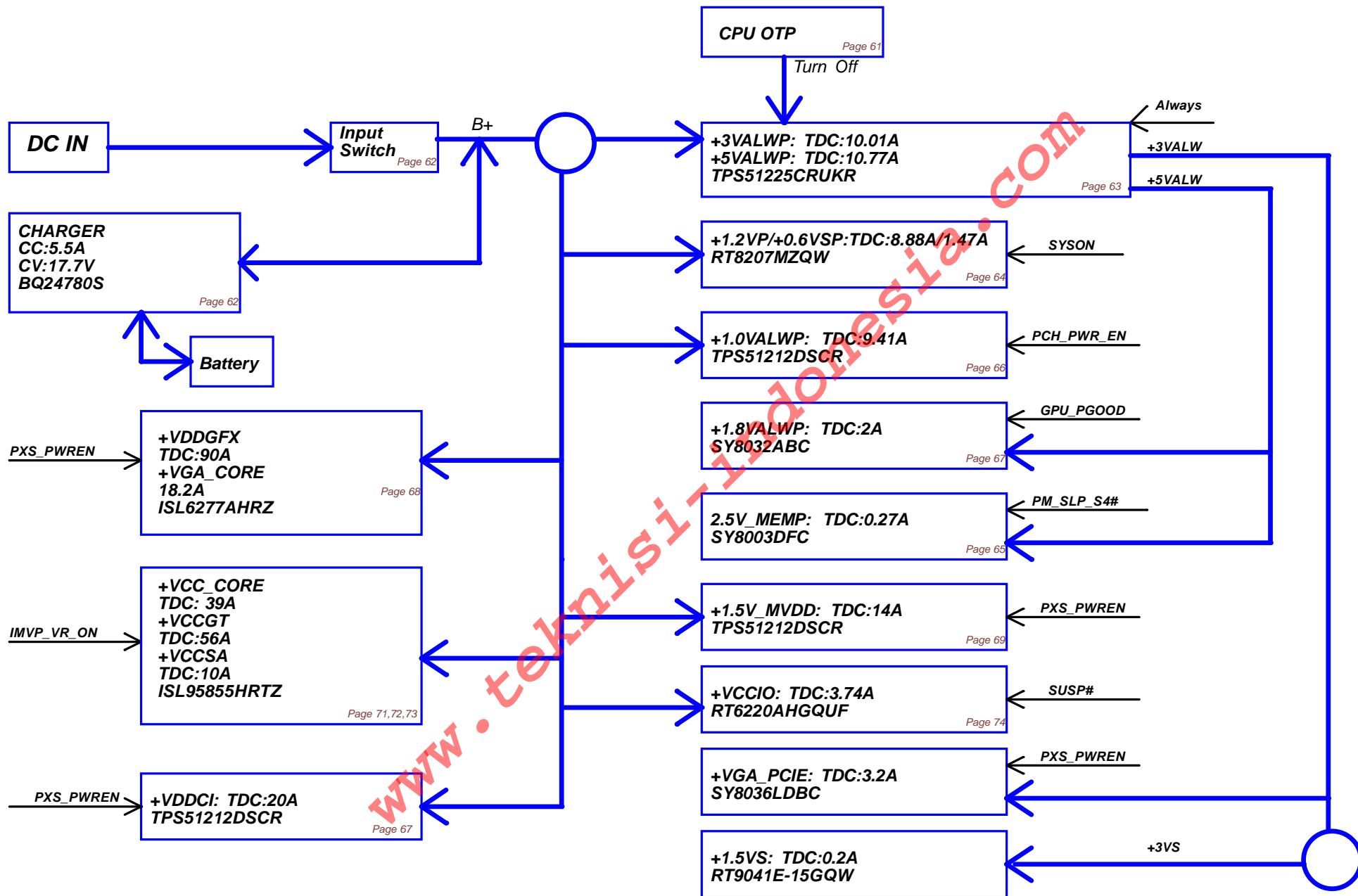


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PROCESSOR DECOUPLING

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# Power block



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	71	PWR_VCORE_ISL95855	2015.4.1	Nick_Lin	Change net from +1.0V_VCCST to +VCCST		
2	71	PWR_VCORE_ISL95855	2015.4.1	Nick_Lin	umount PR5034,PR5035,PR5036,PR5037,PR5038,PR5039	Change from 100_0402_1% (SD034100080) to @ Location:PR5034,PR5035,PR5036,PR5037,PR5038,PR5039	
3	66	PWR_+1VALWP	2015.4.11	Nick_Lin	Change OCP setting	Change from 210K_0402_1%_0402_1% (SD034210380) to 86.6K_0402_1% (SD034866280) Location:PR303	
4	62	PWR_CHARGER	2015.4.11	Nick_Lin	Change PR702 for PMON function	Change from 0.004_1206_1% (SD000017Q00) to 0.005_1206_1%(SD000017R00) Location:PR303	
5	71	PWR_VCORE_ISL95855	2015.4.27	Nick_Lin	Change ISL95855 circuit by FAE advice	Change form SD000009480 (S RES 1/16W 1.47K +-1% 0402) to SD034127180 (S RES 1/16W 1.27K +-1% 0402) Location PR524 Change form SD000009M80 (S RES 1/16W 2.61K +-1% 0402) to SD00000UV00 (S RES 1/16W 3.6K +-1% 0402) Location PR530 Change form SE068221J80 (S CER CAP 220P 25V J NPO 0402) to SE074152K80 (S CER CAP 1500P 50V K X7R 0402) Location PC514 Change form SD034100180 (S RES 1/16W 1K +-1% 0402) to SD000003480 (S RES 1/16W 316 +-1% 0402) Location PR532 Change form SE074681K80 (S CER CAP 680P 50V K X7R 0402) to SE074331K80 (S CER CAP 330P 50V K X7R 0402) Location PC522 Change form SD034100180 (S RES 1/16W 1K +-1% 0402) to SD034453180 (S RES 1/16W 4.53K +-1% 0402) Location PR537 Change form SD034113380 (S RES 1/16W 113K +-1% 0402) to SD034110380 (S RES 1/16W 110K +-1% 0402) Location PR539 Change form SE075223K80 (S CER CAP 0.022U 25V K X7R 0402) to SE076333K80 (S CER CAP .033U 16V K X7R 0402) Location PC530 Change form SD034267080 (S RES 1/16W 267 +-1% 0402) to SD034301080 (S RES 1/16W 301 +1% 0402) Location PR541 Change form SE074222K80 (S CER CAP 2200P 50V K X7R 0402) to SE074471K80 (S CER CAP 470P 50V K X7R 0402) Location PC533 Change form SD034100180 (S RES 1/16W 1K +-1% 0402) to SD034487100 (S RES 1/16W 4.87K +-1% 0402) Location PR511 Change form SE075223K80 (S CER CAP 0.022U 25V K X7R 0402) to SE00000MJ00 (S CER CAP 0.047U 25V K X7R 0402) Location PC517 Change form SE074222K80 (S CER CAP 2200P 50V K X7R 0402) to SE074471K80 (S CER CAP 470P 50V K X7R 0402) Location PC508 Change form SD034182180 (S RES 1/16W 1.82K +-1% 0402) to SD00000UV00 (S RES 1/16W 3.6K +-1% 0402) Location PR521 Change form SD034953280 (S RES 1/16W 95.3K +-1% 0402) to SD034976280 (S RES 1/16W 97.6K +-1% 0402) Location PR500	

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6	71	PWR_VCORE_ISL95855	2015.6.24	Nick_Lin	Change VCC_CORE VR_IMAX	Change form SD034301080 (S RES 1/16W 301 +1% 0402) to SD034442080 (S RES 1/16W 442 +1% 0402) Location PR541 Change form SD034243180 (S RES 1/16W 2.43K +-1% 0402) to SD034357180 (S RES 1/16W 3.57K +-1% 0402) Location PR550 Change form SD034562180 (S RES 1/16W 5.62K +-1% 0402) to SD034280280 (S RES 1/16W 28K +-1% 0402) Location PR517 Change form SD034931280 (S RES 1/16W 93.1K +-1% 0402) to SD034953280 (S RES 1/16W 95.3K +-1% 0402) Location PR548	
7	71	PWR_VCORE_ISL95855	2015.6.24	Nick_Lin	Change VR_ProcH0t Trig point	Change form SD034105280 (S RES 1/16W 10.5K +-1% 0402) to SD000000AJ80 (S RES 1/16W 12.4K +-1% 0402) Location PR545,PR514	
8	61	PWR_DCIN / BATT CONN / OTP	2015.6.24	Nick_Lin	fine tune OTP setting	Change form SD034162280 (S RES 1/16W 16.2K +1% 0402) to SD034147280 (S RES 1/16W 14.7K +1% 0402) Location PR24	

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